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The MSFC Complementary Metal Oxide Semiconductor (Including Multilevel Interconnect Metallization) Process Handbook

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and Donald E. Routh
George C. Marshall Space Flight Center
Marshall Space Flight Center, Alabama

National Aeronautics
and Space Administration

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DEFINITION OF SYMBOLS

Symbol	Definition
B_2O_3	Boron Oxide
BN	Boron Nitride
BV_{DSS}	Drain to Source (Gate Shorted) Breakdown Voltage, V
BV_{GSS}	Gate to Source (Drain Shorted) Breakdown Voltage, V
C_2H_5OH	Ethyl Alcohol
CH_3COOH	Acetic Acid — Glacial
g_m	Transconductance
H_2O	Water
H_3PO_4	Phosphoric Acid
H_2SO_4	Sulfuric Acid
HCl	Hydrochloric Acid
HF	Hydrofluoric Acid
HNO_3	Nitric Acid
I_{DS}	Drain to Source Current, A
I_{DSS}	Drain to Source (Gate Shorted) Leakage Current, A
N+	Heavy Concentration of N-type ions (a relative indication)
N-	Light Concentration of N-type ions (a relative indication)
N_2	Nitrogen Gas
NH_4F	Ammonium Flouride — Crystal

DEFINITION OF SYMBOLS (Continued)

Symbol	Definition
NH_4OH	Ammonium Hydroxide
O_2	Oxygen Gas
P+	Heavy Concentration of P-type ions (a relative indication)
P-	Light Concentration of P-type ions (a relative indication)
PH_3	Phosphine Gas
SiH_4	Silane Gas
SiO_2	Silicon Dioxide
V_{DS}	Drain to Source Voltage, V
V_{FB}	Flatband Voltage, V
V_{GS}	Gate to Source Voltage, V
V_T	Threshold Voltage, V
ΔV_{FB}	Shift of Flatband Voltage, V
ϕ	Phase

STANDARD ABBREVIATIONS

Symbol	Definition
A	ampere
C	celsius
c	centi, 10^{-2}
cm	centimeter
g	gram

DEFINITION OF SYMBOLS (Continued)

Symbol	Definition
Hz	hertz
K	kelvin
k	kilo, 10^3
l	liter
M	mega, 10^6
m	milli, 10^{-3}
m	meter
min	minute
mil	10^{-3} inch
n	nano, 10^{-9}
Pa	pascal
S	siemens
s	second
μ	micro, 10^{-6}
V	volt

NONSTANDARD ABBREVIATIONS

ABS	Alcohol, Brush and Spin Cleaning Procedure
BOE	Buffered Oxide Etchant
CAD	Computer Aided Design

DEFINITION OF SYMBOLS (Continued)

Symbol	Definition
CVD	Chemical Vapor Deposition
C-MOS	Complementary Metal Oxide Semiconductor
DI	Deionized
IC	Integrated Circuit
LSI	Large Scale Integration
LSIC	Large Scale Integrated Circuit
MAX	Maximum
MIN	Minimum
MSFC	George C. Marshall Space Flight Center
MSI	Medium Scale Integration
MSIC	Medium Scale Integrated Circuit
N	Negative
NASA	National Aeronautics and Space Administration
N-MOS	N-channel Metal Oxide Semiconductor
P	Positive
PR	Photoresist
P-MOS	P-channel Metal Oxide Semiconductor
ppm	Parts Per Million
PR2D	Place and Route in Two Dimension

DEFINITION OF SYMBOLS (Concluded)

Symbol	Definition
RT	Room Temperature
rps	Revolutions Per Second
SCr	Sulfuric-Chromic PR Stripper
Silox	SiO_2 CVD System
SP	Sulfuric-Hydrogen Peroxide Cleaner-Stripper
SSI	Small Scale Integration
SSIC	Small Scale Integrated Circuit
STAR	Standard Transistor Array Radix
tds	Total Dissolved Solids
TYP	Typical
UV	Ultraviolet

THE MSFC COMPLEMENTARY METAL OXIDE SEMICONDUCTOR (INCLUDING MULTILEVEL INTERCONNECT METALLIZATION) PROCESS HANDBOOK

SUMMARY

This report presents a description of the fabrication techniques, basic materials used, and other necessary details to create Complementary Metal Oxide Semiconductor (C-MOS) integrated circuits with metal gate. Descriptive information has been included on the multilevel metallization technique and procedure being applied at George C. Marshall Space Flight Center (MSFC). Examples of C-MOS integrated circuits fabricated at MSFC are shown with their functions and applications described. The detailed process is given with single discrete P-MOS and N-MOS transistor configurations. Typical electrical characteristics of both P-MOS and N-MOS discrete devices under given conditions are provided.

Two procedures that can be used in the creation of the P-well necessary for the N-MOS devices are ion implantation and diffusion. Special emphasis is placed on the ion implantation technique since it is the method currently being used at MSFC. Curves of silicon oxidations, boron oxide diffusions, boron nitride diffusions, and SiO_2 etch rates are included. A general description of MSFC design, mask making, packaging, and testing procedures is included.

This report demonstrates the capability of the Electronics Development Division at MSFC in the field of C-MOS microelectronics from conceptual design through final testing, including mask making, fabrication, and packaging. The capabilities described in this report are being utilized in: (1) research and development of new technology, (2) education of individuals in the various disciplines and technologies in the field of microelectronics, and (3) fabrication of many types of specially designed integrated circuits, which are not commercially feasible in small quantities, for many in-house research and development programs.

I. INTRODUCTION

The C-MOS process is a natural extension of the P-MOS process which has been well established in the Design Techniques Branch of the Electronics Development Division of the Electronics and Control Laboratory at MSFC/NASA. The potential of complementary MOS logic is of considerable importance in

aerospace applications and battery operated digital computing equipment in which low power dissipation is one of the prime objectives. Clockrates are, however, generally less than 5 MHz. The art of integrating both P-MOS and N-MOS devices on one chip is an established and exercised process at MSFC. Detailed information helpful in processing either single or double level interconnect metallization has been included. A general description of MSFC design, mask making, packaging, and testing procedures is also provided. Although this report provides an explanation of the procedures from conceptual design to final testing necessary for the fabrication of IC, the process itself is provided in greater detail.

The description of the process, with illustrations included, will aid those unfamiliar with processing to obtain a concept of the work and facilities required to process one of the many types of IC. General descriptions of various other aspects will help complete the overall picture of a complete MOS microelectronics facility.

This report contains the C-MOS process being used at the present time with an explanation of that process. The process itself is presented in great detail to serve as a guide and aid to those attempting to establish a C-MOS process. Included in this report are samples of research and development C-MOS integrated circuits fabricated at MSFC. These examples demonstrate a few of the numerous applications of C-MOS IC's.

II. MICROELECTRONICS CAPABILITY

The Microelectronics facility of the Electronics Development Division possesses the total capability required to create an IC from conceptual design through final testing of the packaged device prior to application. The various steps involved in each of the necessary phases of creating an IC are described in general with the exception of processing. Processing is described in greater detail in later sections of this report.

A. Computer Aided Design

The design and artwork generation phase of the Large Scale Integration (LSI) Computer Aided Design (CAD) System [1] is the first phase in the creation of an IC. To design a Large Scale Integrated Circuit (LSIC), the logic necessary to perform the intended functions must be ascertained. Employing

Boolean algebra, the logic requirements are organized into a logic diagram. Each of the Boolean functions can be performed electrically using a standard cell which performs a given function such as the NAND or the NOR operation. If these standard logic cells are electrically connected in a proper manner, the original logic requirements will be satisfied. From the logic diagram and the Standard Cell Notebook [2], a network interconnection list is developed and punched onto computer cards. A large batch automatic layout (PR2D — Place and Route in Two Dimensions) computer program is executed using these cards as input data. A data base consisting of the layout of the microcircuit with input and output pads, power supply pad, and test devices is formed. This data base is transferred into an interactive graphics computer system [3] and the chip layout is displayed on the face of a cathode ray tube. The designer studies the design in great detail and can make modifications to the design with the graphics system. This data base can also be run as input data into logic simulator computer programs to verify that the logic meets the designer's requirements. If the logic does not, the design phase is repeated until correct.

After the design phase has been completed, the mask artwork must be generated. The automatic layout data are used as inputs into an Artwork Computer Program. This program searches a library which contains all of the mask data for the cells and, with another program, organizes connection patterns and cell shapes into a data format compatible with the mask pattern generation hardware. Before these data, in the form of a magnetic computer tape, are provided to the mask generation facility, the final circuit design is carefully studied using the interactive graphics system to find any design errors. The design phase from conception to artwork generation is generally accomplished in 1 to 3 weeks.

B. Mask Making

The making of photographic masks in the mask generation facility is the second phase in the creation of an IC. In a temperature controlled clean room environment [4], the CAD magnetic tape is loaded onto a computer which transfers the circuit geometry information from the tape into exposures on a high resolution photographic glass plate by means of a pattern generator. This 51 by 51 mm (2 by 2 in.) glass plate containing a magnified (10X) copy of the circuit is then chemically developed. The quality of the circuit image is carefully inspected under a microscope since this glass plate is used as the master from which all circuit patterns on the final mask are reproduced. After inspection, the master is aligned to a metal frame and cleaned. The master is placed in a step and repeat camera system. In this system, the circuit pattern is reduced

by a factor of 10 as it is stepped and repeated in a precise X and Y array. This X and Y array pattern is reproduced onto another 51 by 51 mm (2 by 2 in.) high resolution photographic glass plate that is chemically developed. This final copy is then carefully inspected under a microscope because this plate may be used to contact print additional masks that will be used in the processing phase. In some cases where low volume research and development circuits are to be created, the final step and repeat copies are used directly as they are produced without additional contact printing [5]. In the C-MOS process, seven to nine different masks are used to define the necessary patterns. Each of these must be made individually using the previously described process. Each mask of the set is carefully inspected under a microscope for quality before it is provided to the wafer processing facility. The mask generation phase from magnetic tape to completed set of masks is generally accomplished in 1 week.

C. Wafer Processing

The processing of the silicon wafers into integrated circuits is the third phase in the creation of an IC. The C-MOS process is provided in the next section with a general explanation of the procedures following. Before the wafers are ready to be tested, the wafers are carefully inspected for processing defects. The wafer processing phase from blank silicon wafer to finished circuit is generally accomplished in 2 weeks for one processing run. Multiple runs are sometimes required to create a specific number of properly functioning circuits.

D. Testing

The testing of the finished wafers for electrical and visual quality is the fourth phase in the creation of an IC. Discrete testing is the first test performed. The wafer is held in place on a chuck by a vacuum while small moveable probes are placed on the bonding pads to make electrical connection. The discrete test circuits are used to determine threshold (turn-on) voltage (V_T), drain leakage current (I_{DSS}), drain-source breakdown voltage (BV_{DSS}), and transconductance (g_m). These tests are performed at five positions on the wafer to give an indication of the variation of the parameters across the wafer. The shift of the flatband voltage (ΔV_{FB}) is measured using a capacitance-voltage system which traces curves of capacitance versus voltage before and after the wafers are subjected to elevated temperature and voltage bias. This test indicates the worst-case, long-term V_T shift that should occur. Electrical test parameters are given in the following Table.

TABLE. ELECTRICAL TEST PARAMETERS

Symbol	MIN	TYP	MAX	Units	Conditions
V_T					
P-Channel	-1.0	-1.8	-2.0	V	I_D = -10 μA, V_{DS} = -10 V
N-Channel	+1.0	+1.5	+2.0	V	I_D = +10 μA, V_{DS} = +10 V
I_{DSS}					
P-Channel	(a)	-2.0	-10.0	nA	V_{DS} = -10 V
N-Channel	(a)	+2.0	+10.0	nA	V_{DS} = +10 V
BV_{DSS}					
P-Channel	-30	-32	(b)	V	V_{GS} = 0, I_D = -2 nA
N-Channel	+25	+28	(b)	V	V_{GS} = 0, I_D = +2 nA
g_m (c)					
P-Channel		280	320	μS	V_{DS} = -10 V, I_D = -1 mA
N-Channel		420	460	μS	V_{DS} = 10 V, I_D = 1 mA
ΔV_{FB}	(a)	0.2	0.5	V	Bias = +10 V, 573°K (300°C) 300 s (5 min)
BV_{GSB} (d)	75	100	(b)	V	

(a) Value approaches zero

(b) No upper limit on specification

(c) Width/length ratio assumed to be 6.7

(d) Destructive.

If the discrete devices meet the required specifications, dynamic testing is performed. An algorithm generator and an automated wafer prober are used to measure circuit behavior under simulated operating conditions. This test involves simulating input signals and observing output signals on each circuit. All input combinations are simulated, if possible. The properly functioning circuits are isolated from the defective circuits by the automated wafer prober using an inking technique which marks the defective circuits. The wafer is then scribed with a diamond tipped scribe and rolled to separate the circuits into individual chips or die. The properly functioning chips are then individually cleaned and visually inspected to remove those chips which would have the highest possibility of failure. The testing phase from discrete testing to visual inspection is generally accomplished in 1 week for one processing run.

E. Packaging

The packaging [6] of the functional chips into individual packages is the fifth phase in the creation of an IC. Together with electrical contacts, packaging provides physical and environmental protection to the circuit. A suitable package for the device's application, such as flatpacks, "TO" cans, or dual-in-lines, is chosen for mounting the chip. The chip is attached inside the package by a eutectic or epoxy bonding material. Electrical connections are then made from aluminum bonding pads on the chip to the package's interior leads with small diameter (0.018 to 0.025 mm) gold or aluminum wire. These interconnects are made by either a thermocompression or an ultrasonic wire bonding process. A cover is placed on the package and hermetically sealed. An inert gas, such as nitrogen, is placed inside the package prior to sealing. The time required for the packaging operation varies according to the complexity of the chip, number of wires, and other factors. However, an estimate of 0.25 to 1.0 h per packaged device is typical for low volume, specially designed LSIC.

F. Final Testing

The final testing of the IC is the sixth and final phase in the creation of the IC prior to application. The IC is dynamically tested again using a different electrical connection applicable to the package to eliminate failures due to packaging. The final testing phase is generally accomplished in 1 day for one processing run. The IC is now ready for application.

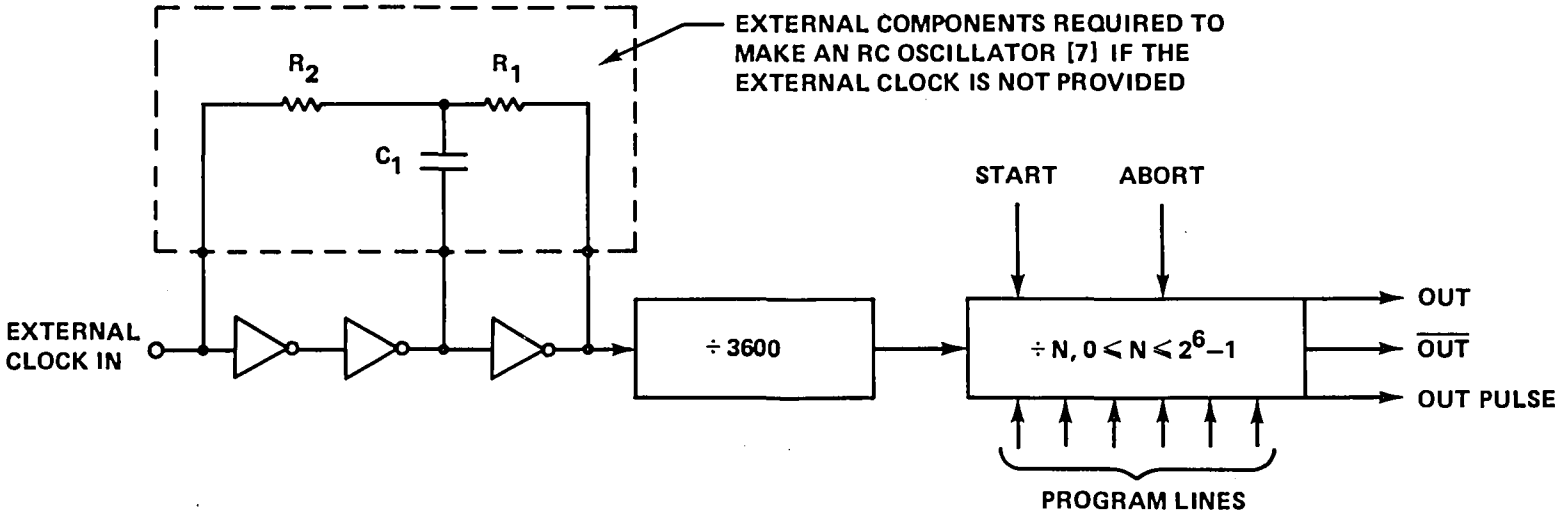
III. EXAMPLES OF APPLICATIONS

A. C-015

C-015 (Figs. 1 and 2) is a programmable (long period) one-shot. An input oscillator (either EXTERNAL CLOCK or internal oscillator) establishes an input time period. This time period is then multiplied (i.e., the frequency is divided) by 3600. If, for example, a 60-Hz input frequency is used, then the output of the ÷3600 stage has a period of 1 min. The ÷N stage divides this input by N, where N is between 0 and 2^6-1 and is selected by a binary code of ones and zeros (V_{DD} and ground respectively) on the program lines. So with a 60-Hz input, the output is N × (1 min), where N is between 0 and 63. That is the output, for a 60-Hz input, ranges from 0 to 63 min with 1 min resolution. In use, the OUT line is normally low, NOT OUT is normally high, and OUT PULSE is normally low. A high-to-low transition on the START line causes OUT to go high and NOT OUT to go low for the preselected time period. On the last half cycle of the input oscillator, OUT PULSE goes high. On the high-to-low transition of the end of the last cycle of the input oscillator, OUT PULSE goes low, OUT goes low, and NOT OUT goes high. This is the end of the time period. START is ignored during the timing period; ABORT is ignored during the idle period; and Program lines are ignored during the timing period. A high-to-low transition on the ABORT line during a timing period ends that timing period with OUT PULSE, OUT, and NOT OUT behaving as in a normal end of a time period.

B. C-016

C-016 (Figs. 3 and 4) is a programmable, retriggerable (long period) one-shot. It performs much like C-015 except that OUT PULSE and ABORT are not available. In their places are START + OUT and NOT(START + OUT). In addition, START is not ignored during a timing period. Instead, a high-to-low transition on the START line at any time begins a timing period. That is, if a timing period is in progress (i.e., OUT is high, NOT OUT is low), a high-to-low transition on the START line reinitiates a timing period without changing the states of OUT or NOT OUT. (Because of this, the program data for a retriggered time period will be the same as for the previous time period because the program lines are read only when OUT goes from low to high and OUT remains high during retriggering.) The purpose of the START + OUT and NOT(START + OUT) lines is to provide a minimum time period for a device controlled by the START line. If a device should be on for a minimum of 5 min, for example, and START may be high for much less than 5 min, then using START + OUT (with program lines set to five with a 60-Hz input) to the circuit will assure a minimum of 5 min "on" time for the device.



$$f \approx \frac{1}{2R_1C_1\left(\frac{0.405\,R_2}{R_1+R_2}+0.693\right)}$$

Figure 1. C-015 block diagram.

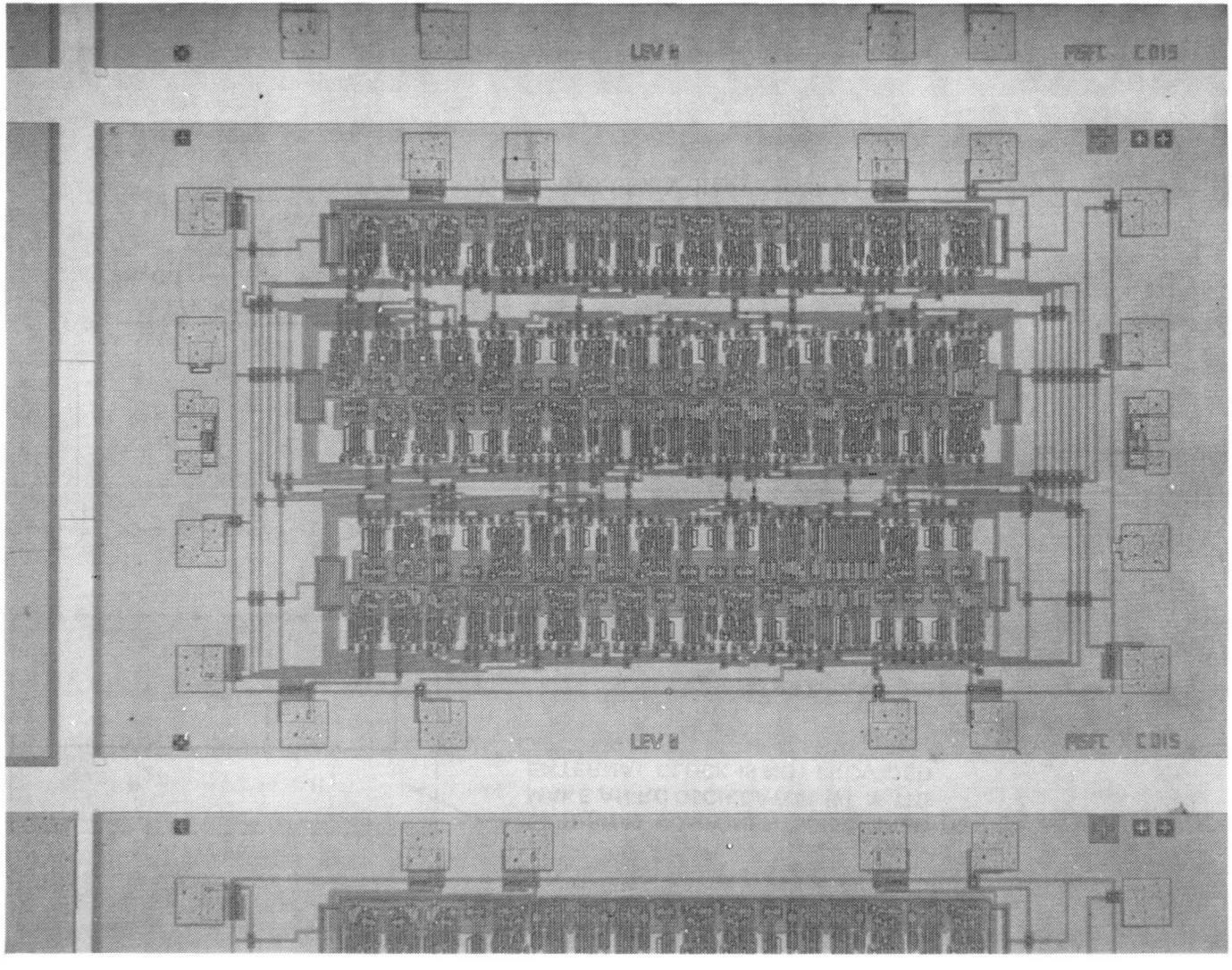
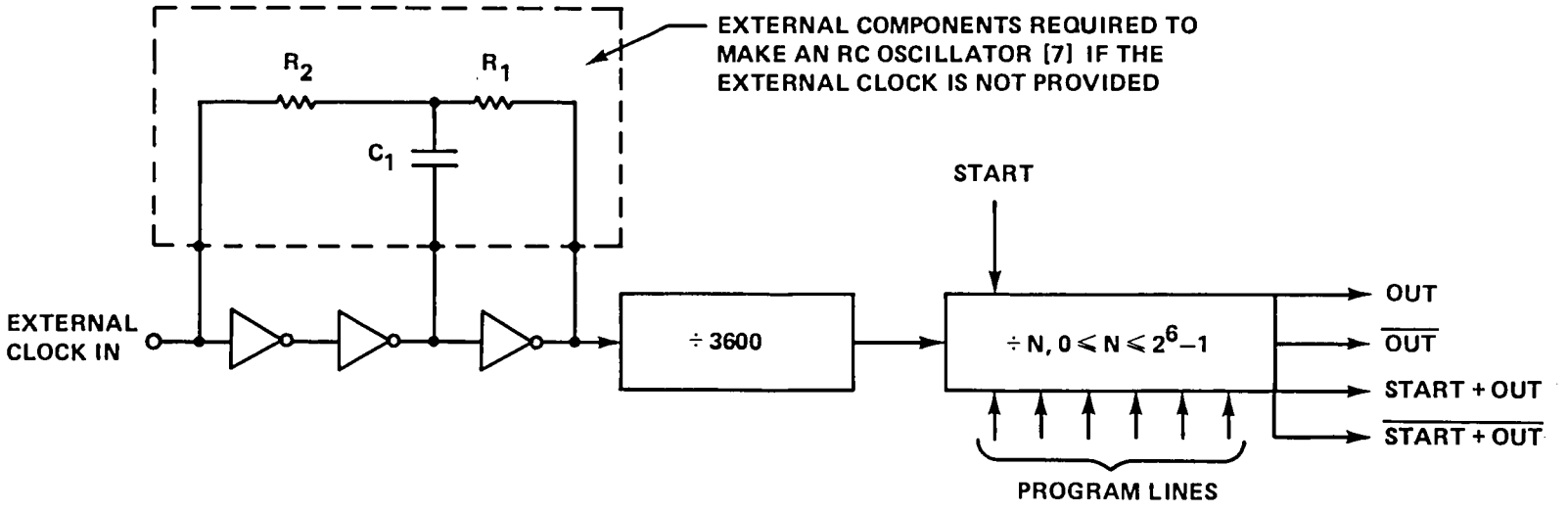


Figure 2. C-015 device chip.



$$f \approx \frac{1}{2R_1C_1\left(\frac{0.405\,R_2}{R_1+R_2}+0.693\right)}$$

Figure 3. C-016 block diagram.

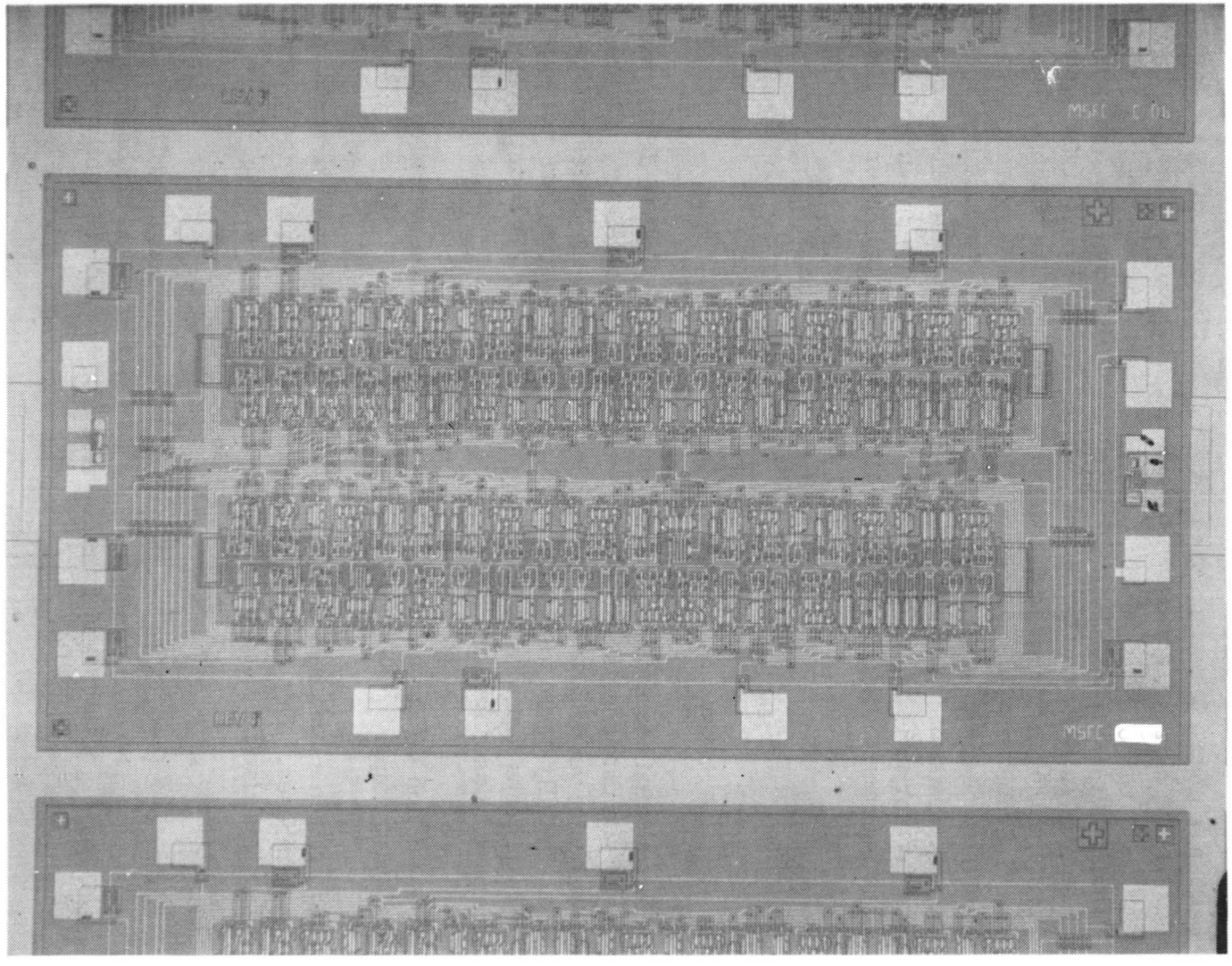


Figure 4. C-016 device chip.

C. STAR

STAR (Fig. 5) is an acronym for Standard Transistor Array Radix, which means the circuit has a standard structure of transistors upon which a custom metal pattern is placed to produce the desired circuit by connecting the needed transistors. The MSFC STAR is being made in double metal.

This particular STAR circuit, designated SC101, contains approximately 384 devices plus discrete test transistors. This circuit is part of the decision-making circuitry for a controller used in a demonstration solar house. The inputs to the circuit consist of four inputs which are clocked in through flip-flops, a clock, and two static inputs. The outputs are derived from combinational logic circuitry and consist of four unique outputs and three outputs which are derived by "ORing" two or three of the four unique outputs. Two of the four unique outputs are fed back through internal flip-flops into the combinational logic circuitry.

IV. C-MOS PROCESS

This section presents our C-MOS double metal process in detail, with examples of test data sheets and notes of in-process measurement. Figures 6 through 31 depict the condition of both the test wafers and the device wafers after each step. Initially seven wafers are used. Three of these wafers are to be used for in-process test wafers (identified as #1, #2, and #7) with the remaining four wafers to be used for active device wafers.

See Section V (Explanation of C-MOS Process) for a narrative on each of the following steps.

Note: After each numbered step of the process, a notation will be found in parentheses. This notation provides the wafers to be affected by this step and also the condition of the test wafer at the beginning of this step.

Example: (1-6, 1,2 (N-) no oxide) Wafers 1 through 6 will go through this step. Test wafers 1 and 2 (at the beginning of this step) have no oxide on them and are lightly doped N material.

Note: Typical exposure times, etch times, and some test values have been provided, these are for reference purposes only.

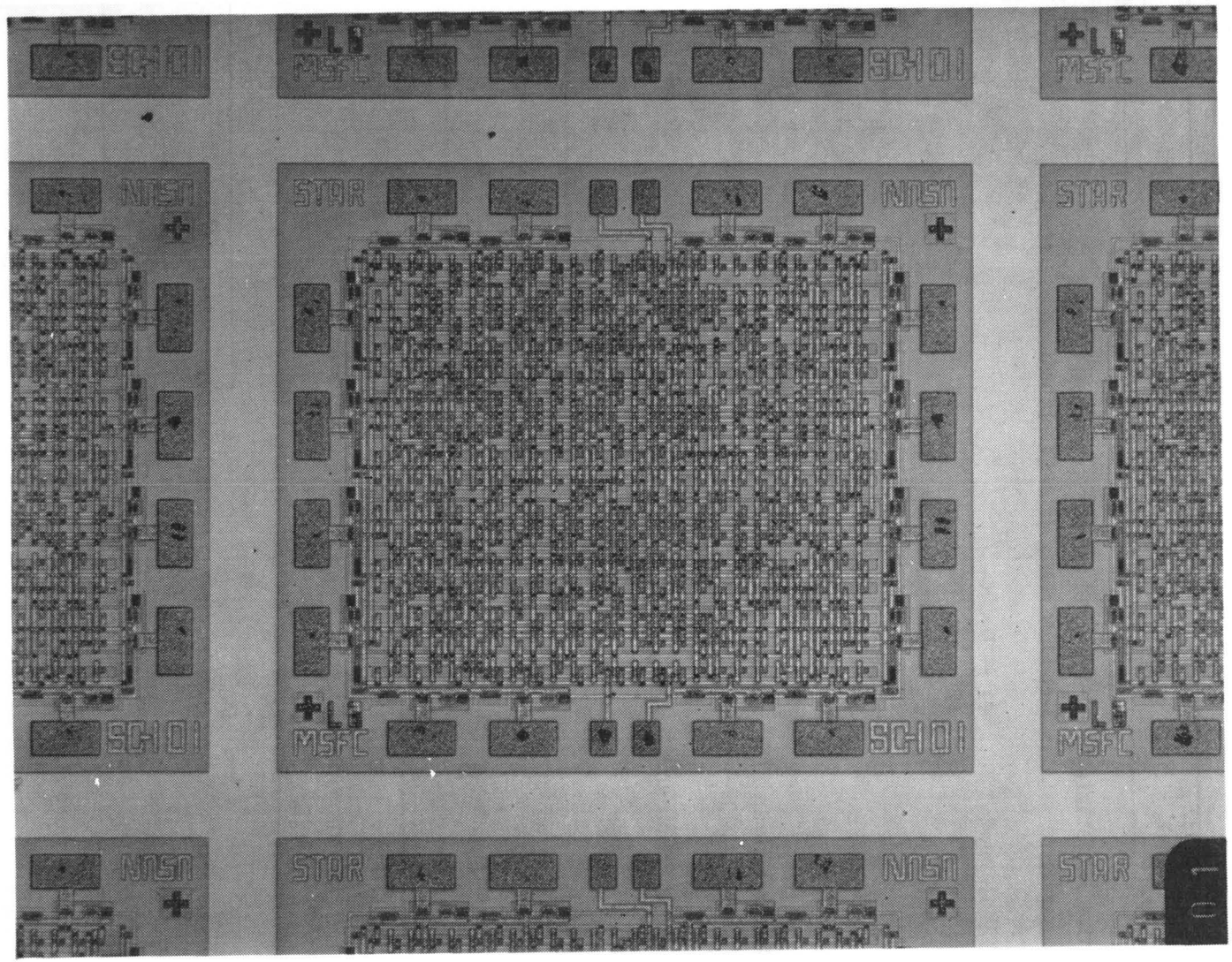


Figure 5. STAR device chip.

C-MOS BULK Si DOUBLE METAL

Process: 6-13-78

Mask I.D.: _____ Processor: _____

Run I.D.: _____ Date: _____

Starting Material: N-type, Phosphorous doped Si
5-8 Ohm-cm, <100> Orientation

Test Wafers: #1 — P-/N-
#2 — N+/P-/N-
#7 — P+/N-

A. FIRST OXIDE

1. Initial clean (Fig. 6)
(1-6, 1,2(N-) no oxide)

   a. ABS clean

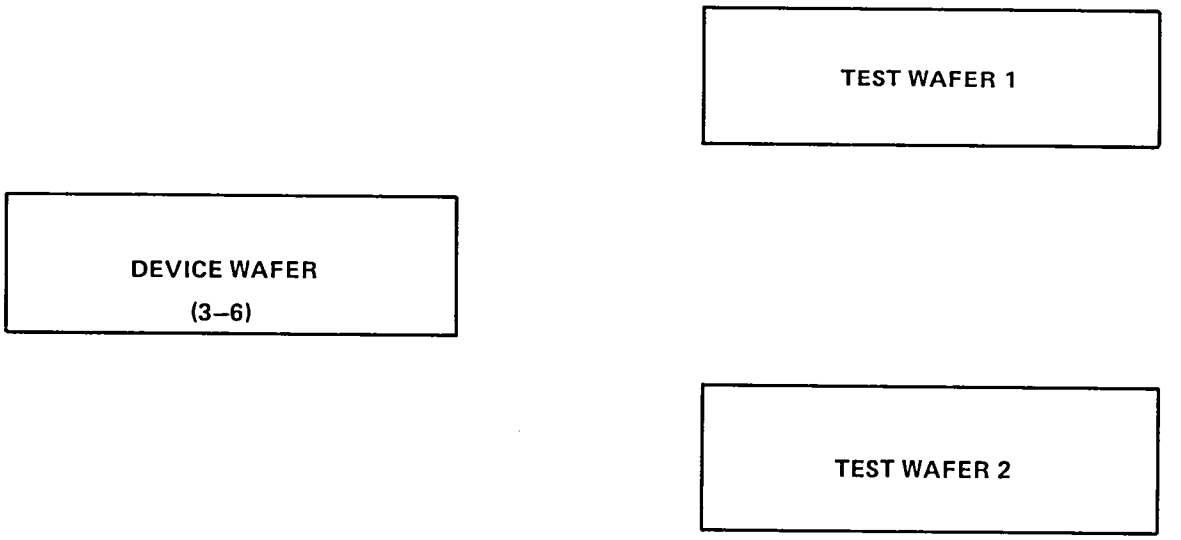


Figure 6. Silicon wafer after initial clean

2. First oxidation 600 nm (Fig. 7) 1423°K (1150°C) 50 mm tube
(1-6, 1,2(N-) no oxide)

a.	O_2	13.6 cm^3/s 300 s (5 min)
b.	H_2O (boiling)	3600 s (60 min)
c.	O_2	13.6 cm^3/s 900 s (15 min)
d.	N_2	31 cm^3/s 1200 s (20 min)

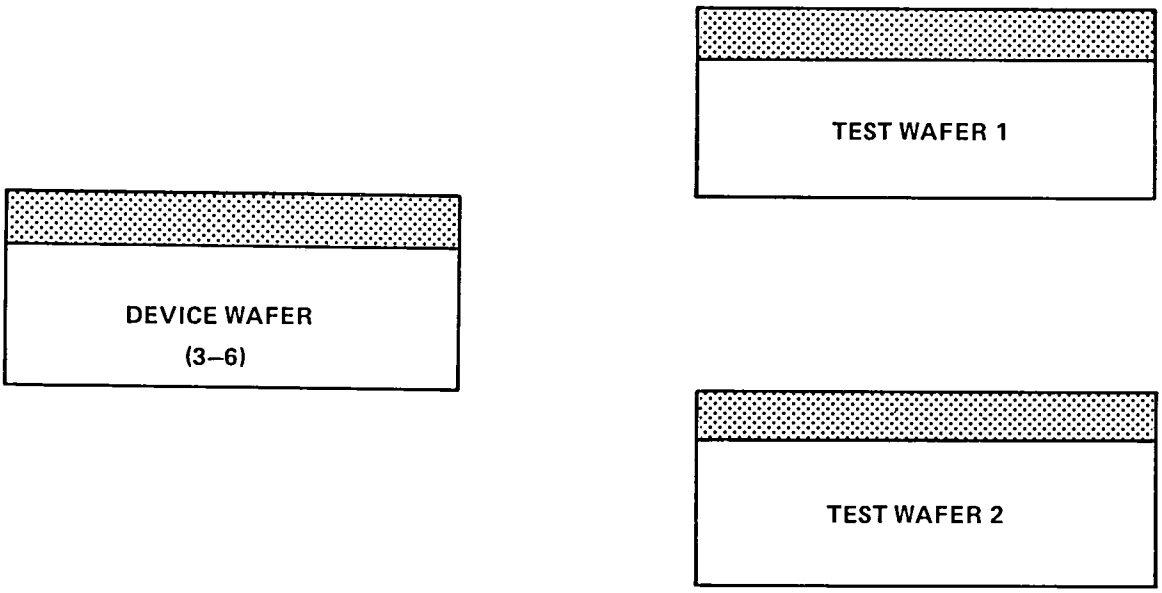


Figure 7. Initial oxidation.

B. P-WELL ION IMPLANTATION

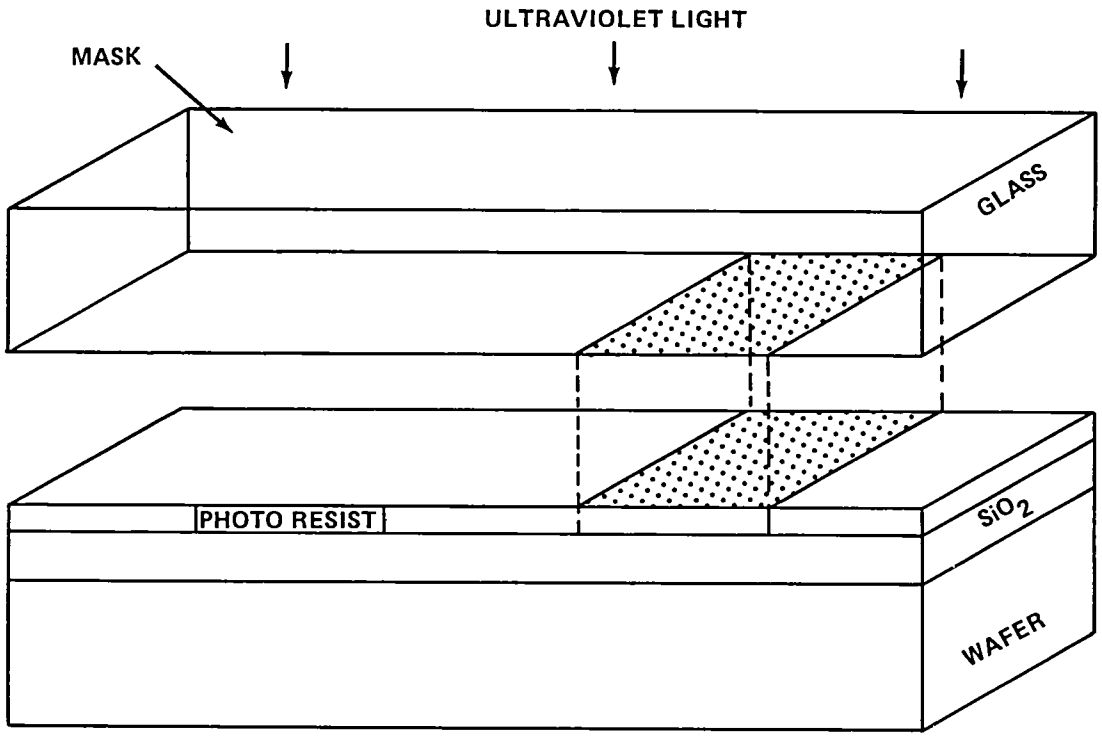
1. PR with Mask 1 (Fig. 8)
(3-6, first oxide)

a.	Apply PR	
b.	Spin at 100 rps	15 s
c.	Prebake in N_2 at 333°K (60°C)	1800 s (30 min)
d.	Align Mask 1	
e.	Expose with UV light 12 mJ/cm^2	t = (2-4) s

f.	Spray develop with PR developer	15 s
g.	Spray rinse with PR rinse	15 s
h.	Spin dry at 100 rps	15 s
i.	Postbake in N_2 at 413°K (140°C)	1800 s (30 min)

1. PR WITH MASK

a. APPLY PR	
b. SPIN AT 100 RPS	15 s
c. PREBAKE IN N_2 AT 343°K (70°C)	1800 s (30 MIN)
d. ALIGN MASK 1	
e. EXPOSE WITH ULTRAVIOLET (UV) LIGHT	8 X



f. SPRAY DEVELOP WITH PR DEVELOPING SOLUTION	15 s
g. SPRAY RINSE WITH PR RINSING SOLUTION	15 s
h. BLOW DRY WITH N_2	
i. POSTBAKE IN N_2 AT 413°K (140°C)	1800 s (30 MIN)

Figure 8. Typical photoresist step.

2. P-Well etch (Fig. 9)
(1-6, 1,2(N-) first oxide)

a. Etch #1,2 in BOE at RT	$t = \frac{(300\text{-}420)}{t + 15}$ s
b. Etch #3-6 in BOE at RT	
c. Rinse in H_2O	600 s (10 min)

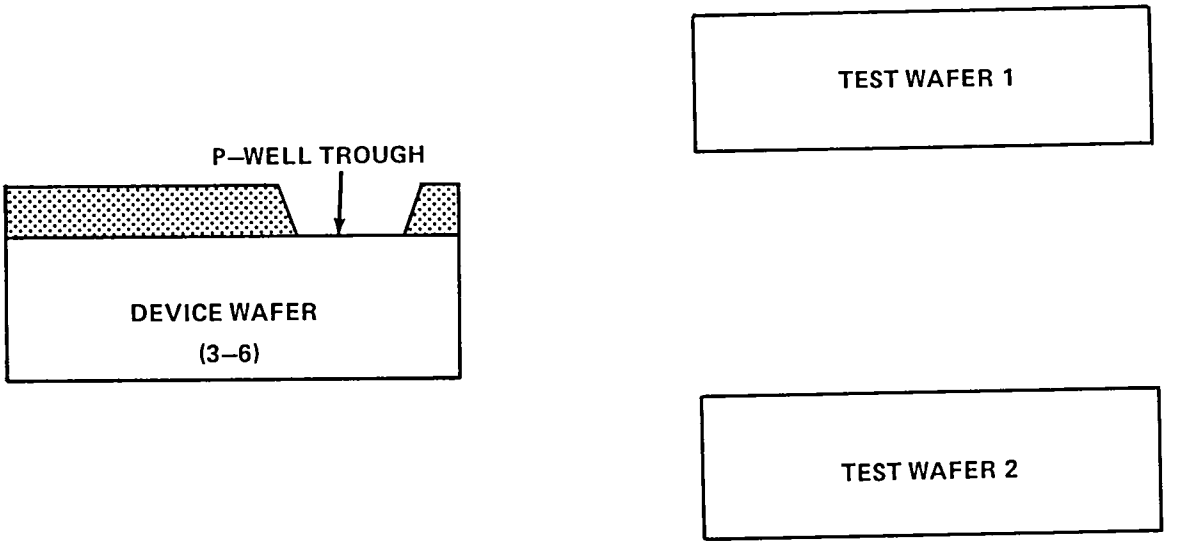


Figure 9. P-Well cutout.

3. PR strip
(3-6)

a. Strip PR in SP solution (freshly mixed)	300 s (5 min)
b. Rinse in H_2O	600 s (10 min)
c. Blow dry with N_2	

4. Implant oxide 50 nm (Fig. 10) 1423°K (1150°C) 50 mm tube
(1-6, 1,2(N-) no oxide)

a. O_2	13.6 cm^3/s 600 s (10 min)
b. N_2	31 cm^3/s 900 s (15 min)

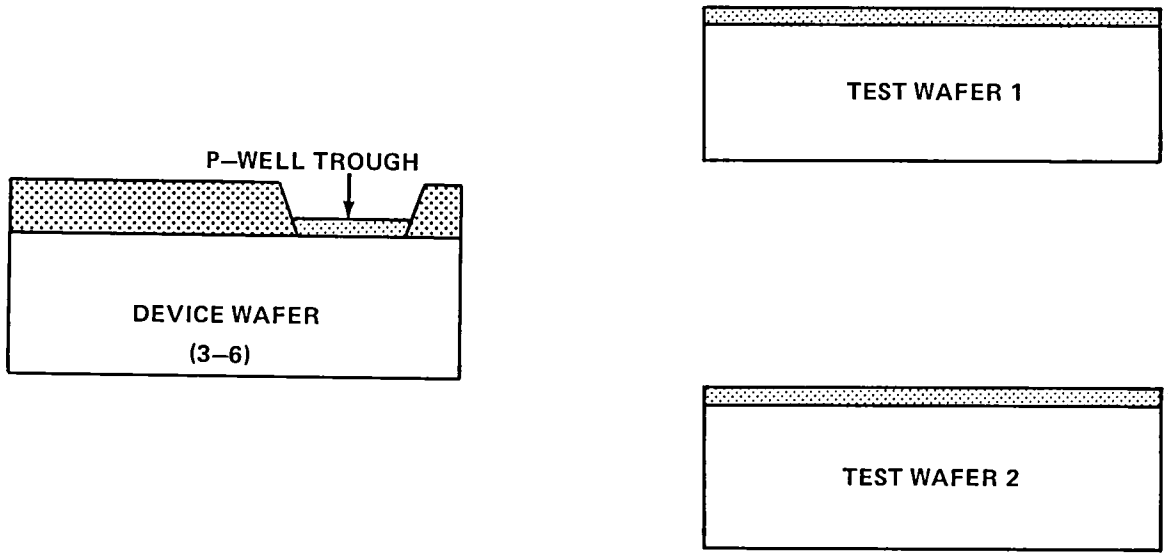


Figure 10. P-Well protective oxide.

5. Ion implantation 2.5 $(10^{13})/cm^2$ (Fig. 11)
(1-6, 1,2(N-) implant oxide)

a. Implant at 120 keV t = (12-15) s

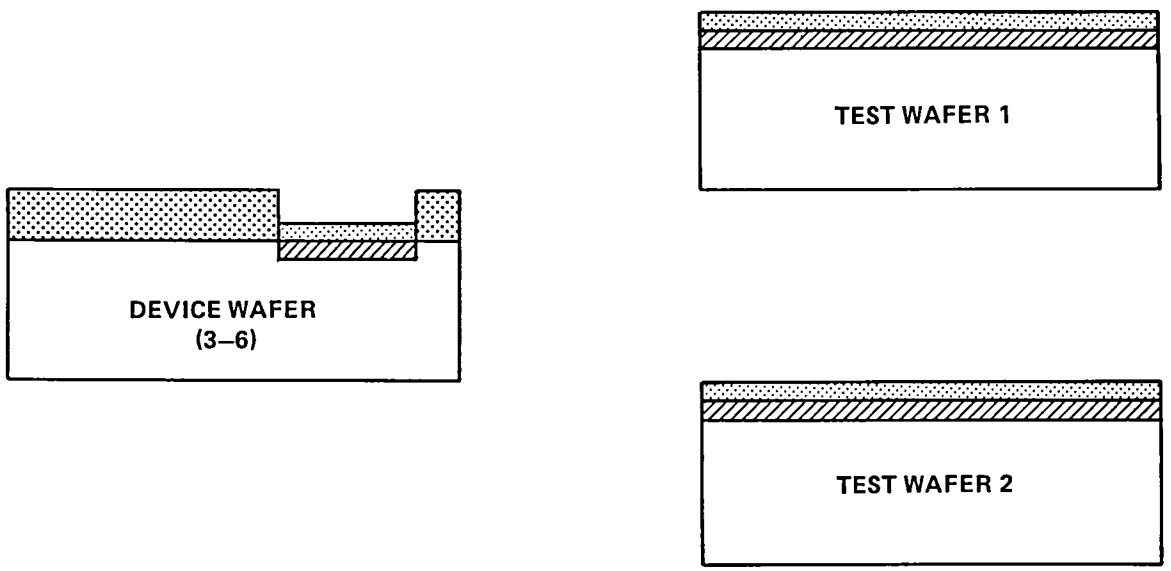


Figure 11. P-Well after ion implantation.

6. Oxide strip (Fig. 12)
(1-6, 1,2(P-/N-) implant oxide)

a. Etch #1-6 in BOE to Si at RT — $t = \frac{(300\text{-}420)}{600\ s\ (10\ min)}\ s$
b. Rinse in H_2O
c. Blow dry with N_2

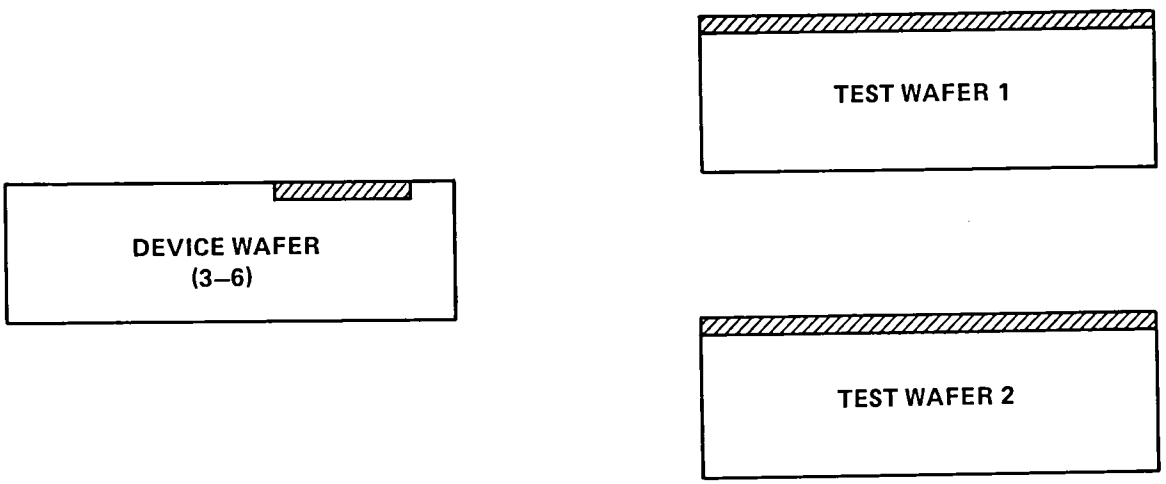


Figure 12. P-Well before drive-in.

7. Wafer #7 preparation
(7(N-) no oxide)

a. ABS clean

8. Drive-in 520 nm (Fig. 13) 1423°K (1150°C) 50 mm tube
(1-7, 1,2(P-/N-), 7(N-) no oxide)

a. O_2 13.6 cm^3/s 57600 s (16 h)
b. N_2 31 cm^3/s 1800 s (30 min)

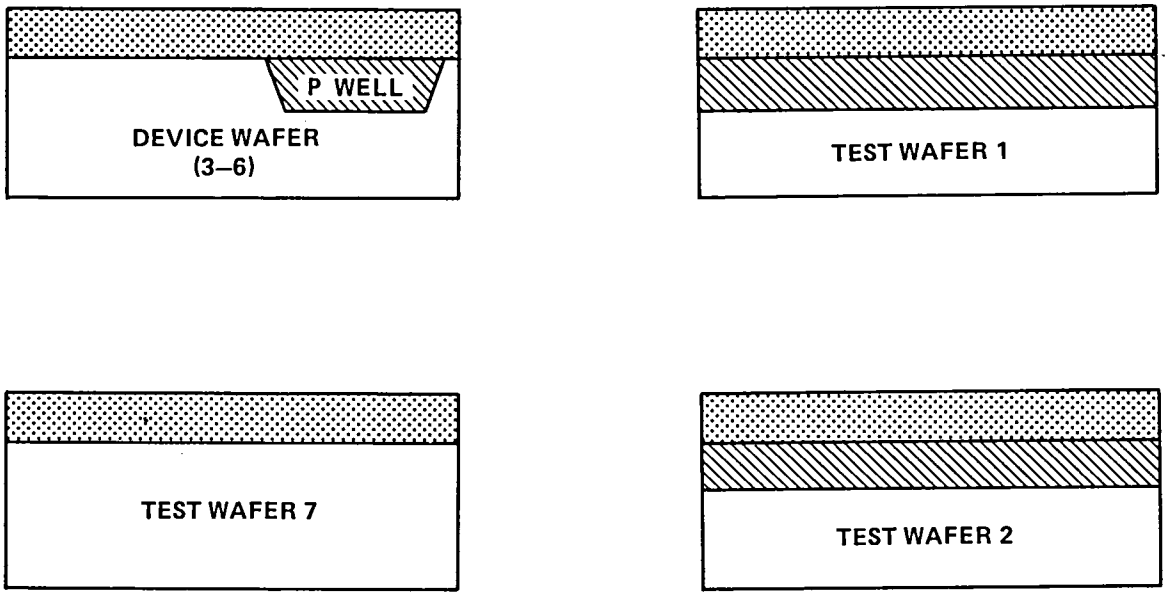


Figure 13. P-Well after drive-in.

C. P+ BORON DIFFUSION

1. PR with Mask 2
   (3-6)

a. Apply PR	
b. Spin at 100 rps	15 s
c. Prebake in N_2 at 333°K (60°C)	1800 s (30 min)
d. Align Mask 2	
e. Expose with UV light 12 mJ/cm^2	t = (2-4) s
f. Spray develop with PR developer	15 s
g. Spray rinse with PR rinse	15 s
h. Spin dry at 100 rps	15 s
i. Postbake in N_2 at 413°K (140°C)	1800 s (30 min)

2. P+ boron diffusion etch (Fig. 14)
   (3-7, 7(N-) P-well oxide)

a. Etch #7 in BOE at RT	t = (300-420) s
b. Etch #3-6 in BOE at RT	t+15 s
c. Rinse in H_2O	600 s (10 min)

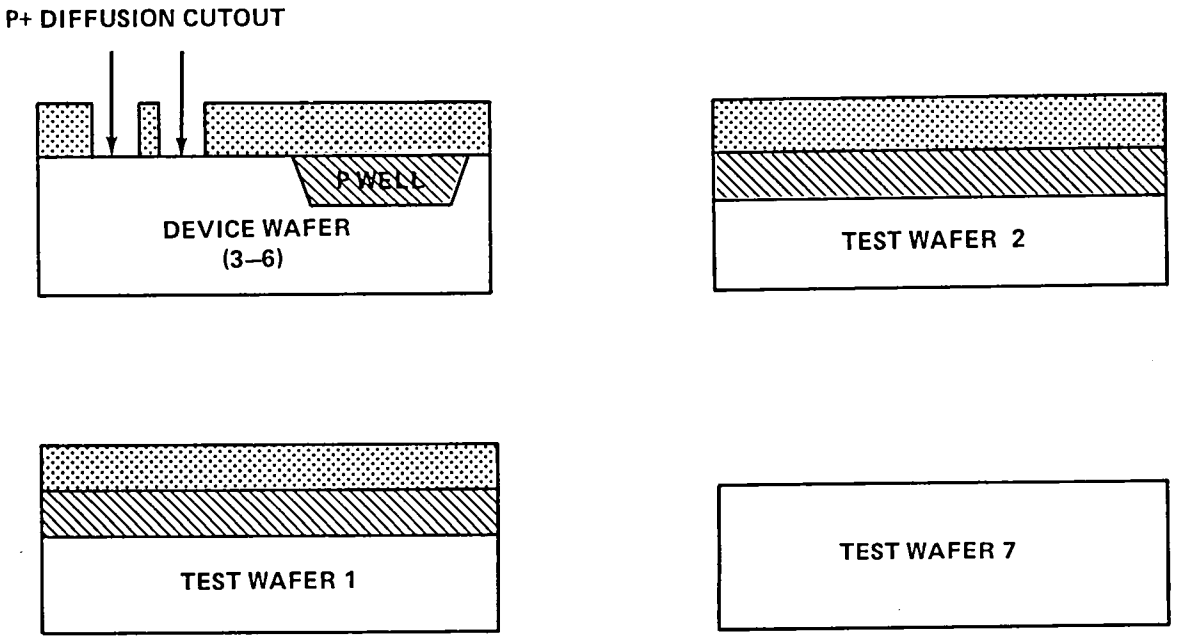


Figure 14. P+ diffusion cutout.

3. PR strip
(3-6)

a. Strip PR in SP solution (freshly mixed)	300 s (5 min)
b. Rinse in H_2O	600 s (10 min)
c. Blow dry with N_2	

4. P+ boron diffusion (Fig. 15) 1253°K (980°C) 74 mm tube
(3-7, 1,2(P-/N-) P-well oxide, 7(N-) no oxide)

a. N_2 (B_2O_3 source)	17 cm^3/s 2400 s (40 min)

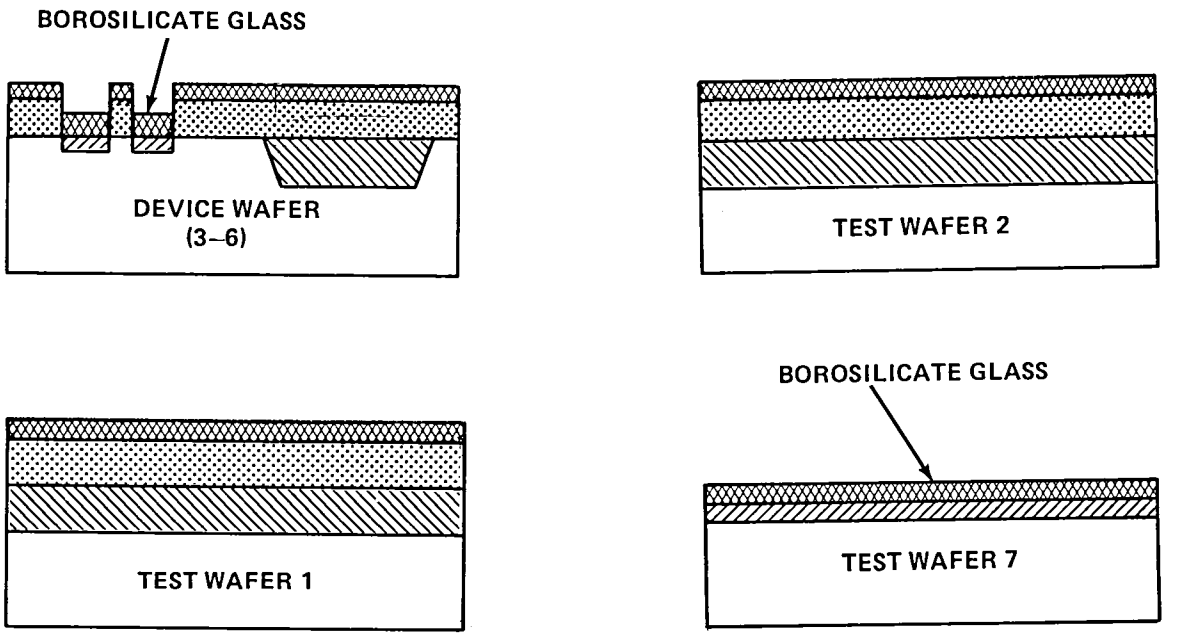


Figure 15. Boron P+ diffusion.

5. Borosilicate glass removal (Fig. 16)
(1-7, 1,2(P-/N-) boron glass over P-well oxide,
7 (P+/N-) boron glass)

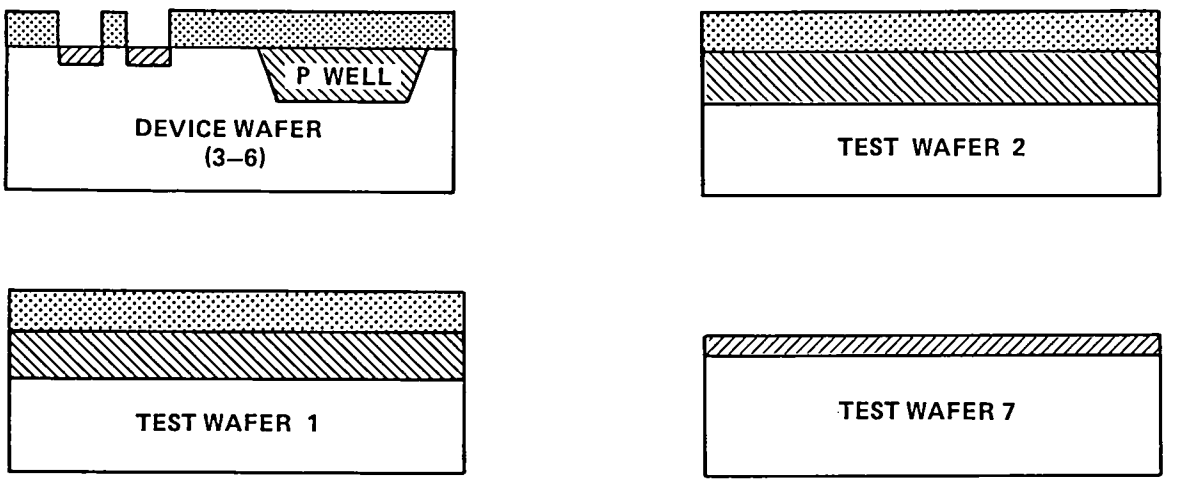


Figure 16. Borosilicate glass and oxide mask removal.

a. Etch #1-7 in BOE at RT 60 s (1 min)
b. Rinse in H_2O 300 s (5 min)
c. Etch #1-7 in Jacobson's etchant at 368°K (95°C) 3600 s (60 min)

d. Rinse in H_2O 600 s (10 min)
e. Etch #1-7 in BOE at RT 60 s (1 min)
f. Rinse in H_2O 600 s (10 min)
g. Blow dry with N_2

6. Resistivity check
(7(P+/N-) 25-35 Ω /□)

a. Measure R_s of #7

1: _____ 2: _____ 3: (25-32) 4: _____ 5: _____

D. N+ MASKING OXIDE

1. N+ masking oxide 200 nm (Fig. 17) 1173°K (900°C) 50 mm tube
(1-7, 1,2(P-/N-) P-well oxide, 7(P+/N-) no oxide)

a. O_2 28 cm^3/s 300 s (5 min)
b. H_2O (boiling) 3600 s (60 min)
c. O_2 28 cm^3/s 900 s (15 min)
d. N_2 31 cm^3/s 1200 s (20 min)

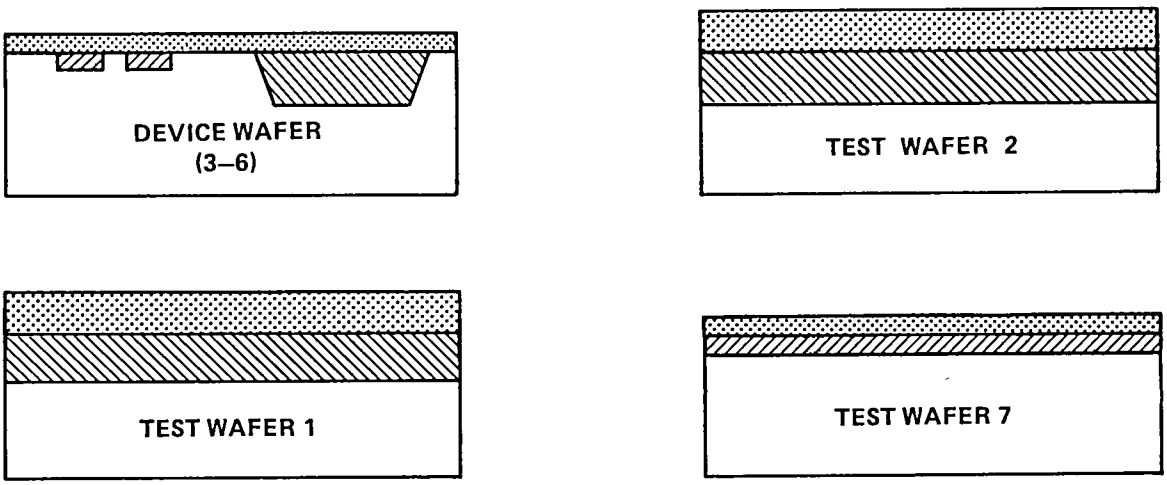


Figure 17. Grow N+ masking oxide.

E. N+ PHOSPHOROUS DIFFUSION

1. PR with Mask 3
(3-6)

a.	Apply PR	
b.	Spin at 100 rps	15 s
c.	Prebake in N_2 at 333°K (60°C)	1800 s (30 min)
d.	Align Mask 3	
e.	Expose with UV light 12 mJ/cm^2	t = (2-4) s
f.	Spray develop with PR developer	15 s
g.	Spray rinse with PR rinse	15 s
h.	Spin dry at 100 rps	15 s
i.	Postbake in N_2 at 413°K (140°C)	1800 s (30 min)

2. N+ phosphorous diffusion etch (Fig 18)
(2-6, 2(P-/N-) P-well oxide)

a.	Etch #2 in BOE at RT	t = (300-420) s
b.	Etch #3-6 in BOE at RT	t+15 s
c.	Rinse in H_2O	600 s (10 min)

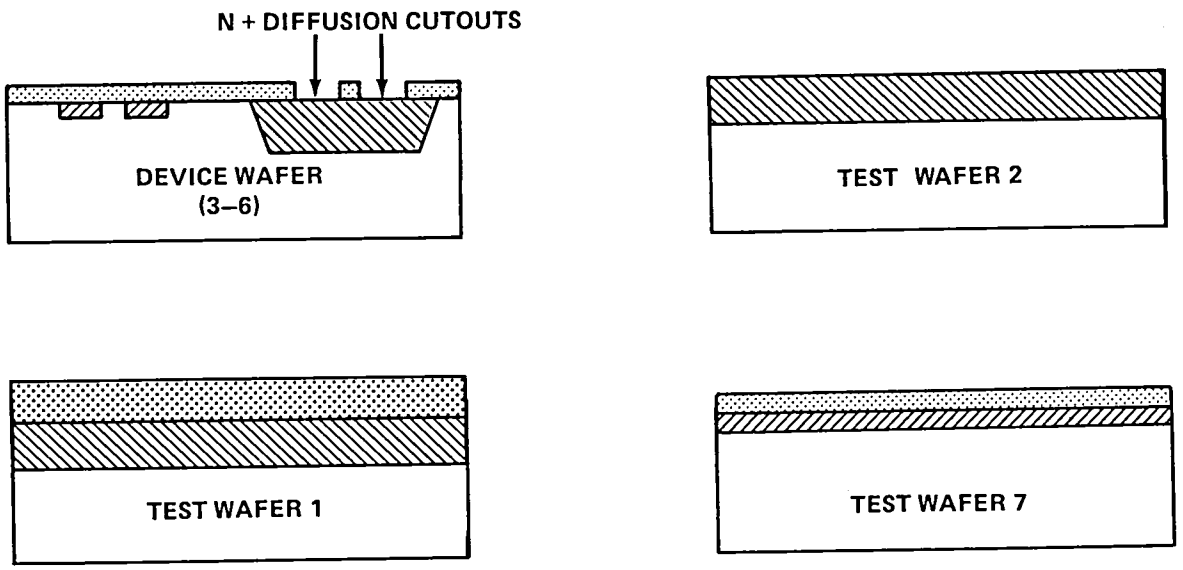


Figure 18. N+ diffusion cutout.

3. PR strip
(3-6)

a.	Strip PR in SP solution (freshly mixed)	300 s (5 min)
b.	Rinse in H_2O	600 s (10 min)
c.	Blow dry with N_2	

4. Resistivity check
(2(P-/N-) 2000-2200 Ω /□)

a. Measure R_s of #2

1: _____ 2: _____ 3: (2000-2200) 4: _____ 5: _____

5. N+ phosphorous diffusion (Fig. 19) 1253°K (980°C) 74 mm tube
(1-7, 1(P-/N-) P-well oxide, 2(P-/N-) no oxide,
7(P+/N-) N+ mask oxide)

a. O_2	7.5 cm^3/s
N_2	15 cm^3/s 300 s (5 min)
b. O_2	7.5 cm^3/s
N_2	15 cm^3/s
PH_3 (1% in Ar)	3.9 cm^3/s 900 s (15 min)
c. O_2	7.5 cm^3/s
N_2	15 cm^3/s 300 s (5 min)

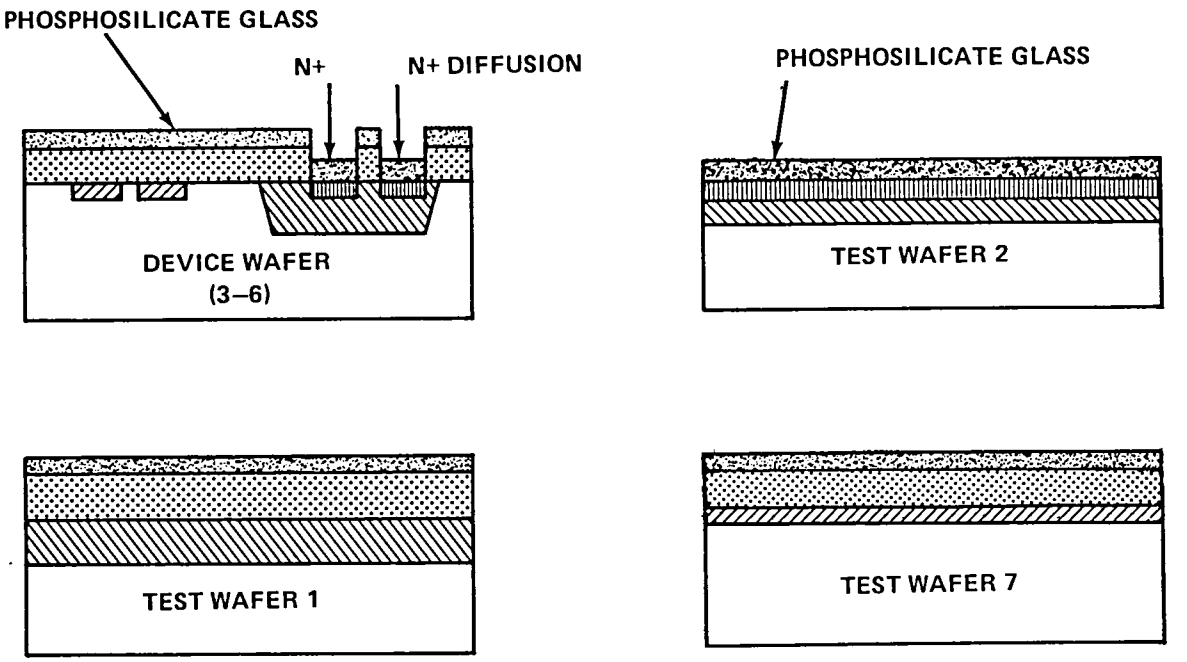


Figure 19. Phosphorus N+ diffusion.

F. FIELD OXIDE

1. Strip oxide (Fig. 20)
   (1-7, 1(P-/N-) phosphorous glass over P-well oxide,
   2(N+/P-/N-) phosphorous glass,
   7(P+/N-) phosphorous glass over N+ masking oxide)

   a. Etch #1-7 in BOE to Si at RT — $t = \frac{(300\text{-}420)}{600\ \text{s}\ (10\ \text{min})}$ s
   b. Rinse in H_2O
   c. Blow dry with N_2

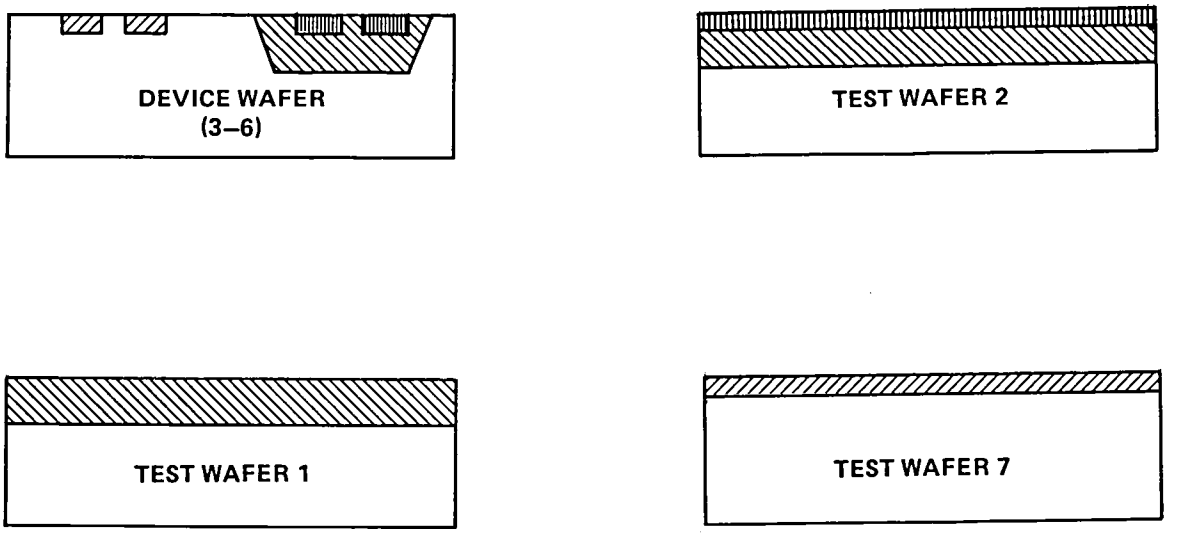


Figure 20. Phosphosilicate glass removal.

2. Resistivity check
   (1(P-/N-) 2000-2200 Ω /□, 2(N+/P-/N-) 15-25 Ω /□, 7(P+/N-) 50-100 Ω /□

   a. Measure R_S of #1

      1: _____ 2: _____ 3: (2000-2200) 4: _____ 5: _____

   b. Measure R_S of #2

      1: _____ 2: _____ 3: (15-20) 4: _____ 5: _____

   c. Measure R_S of #7

      1: _____ 2: _____ 3: (80-100) 4: _____ 5: _____

3. Field oxidation 400 nm (Fig. 21) 1173°K (900°C) 50 mm tube
(1-7, 1(P-/N-), 2(N+/P-/N-), 7(P+/N-) no oxide)

a. O_2	28 cm^3/s 300 s (5 min)
b. H_2O (boiling)	3600 s (60 min)
c. O_2	28 cm^3/s 900 s (15 min)
d. N_2	31 cm^3/s 1200 s (20 min)

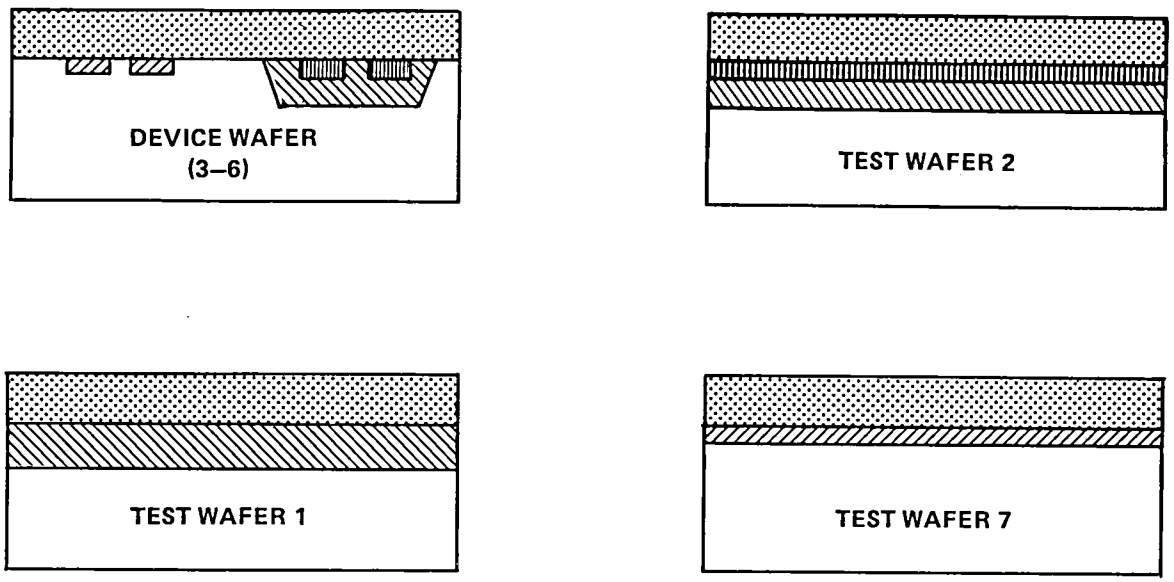


Figure 21. Grow field oxide.

G. GATE OXIDE

1. PR with Mask 4
(3-6, field oxide)

a. Apply PR	
b. Spin at 100 rps	15 s
c. Prebake in N_2 at 333°K (60°C)	1800 s (30 min)
d. Align Mask 4	
e. Expose with UV light 12 mJ/cm^2	t = (2-4) s
f. Spray develop with PR developer	15 s
g. Spray rinse with PR rinse	15 s
h. Spin dry at 100 rps	15 s
i. Postbake in N_2 at 413°K (140°C)	1800 s (30 min)

2. Gate oxide etch (Fig. 22)
(1-7, 1(P-/N-), 2(N+/P-/N-), 7(P+/N-) field oxide)

a. Etch #2, 7, 1 in BOE at 323°K (50°C) t = (40-60) s
b. Etch #3-6 in BOE at 323°K (50°C) t+5 s
c. Rinse in H_2O 600 s (10 min)

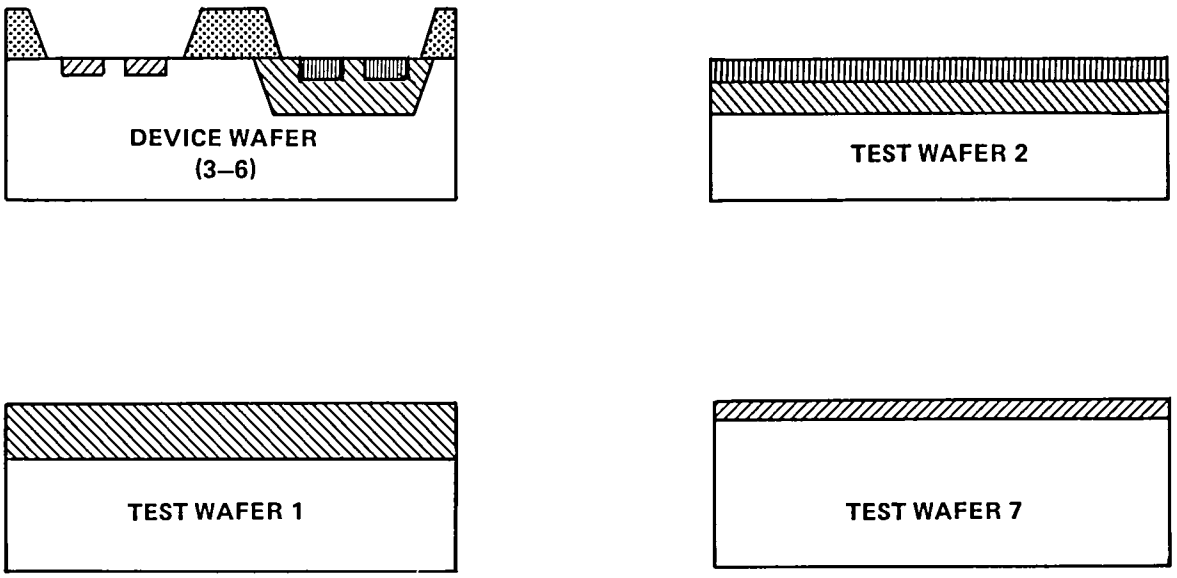


Figure 22. Gate cutout.

3. PR strip
(3-6)

a. Strip PR in SP solution (freshly mixed) 300 s (5 min)
b. Rinse in H_2O 600 s (10 min)
c. Blow dry with N_2

4. Gate oxidation 130 nm (Fig. 23) 1173°K (900°C) 50 mm tube
(1-7, 1(P-/N-), 2(N+/P-/N-), 7(P+/N-) no oxide)

a. O_2 28 cm^3/s 300 s (5 min)
b. HCl:H_2O (azeotropic, boiling) 3600 s (60 min)
c. O_2 28 cm^3/s 900 s (15 min)
d. N_2 31 cm^3/s 1200 s (20 min)

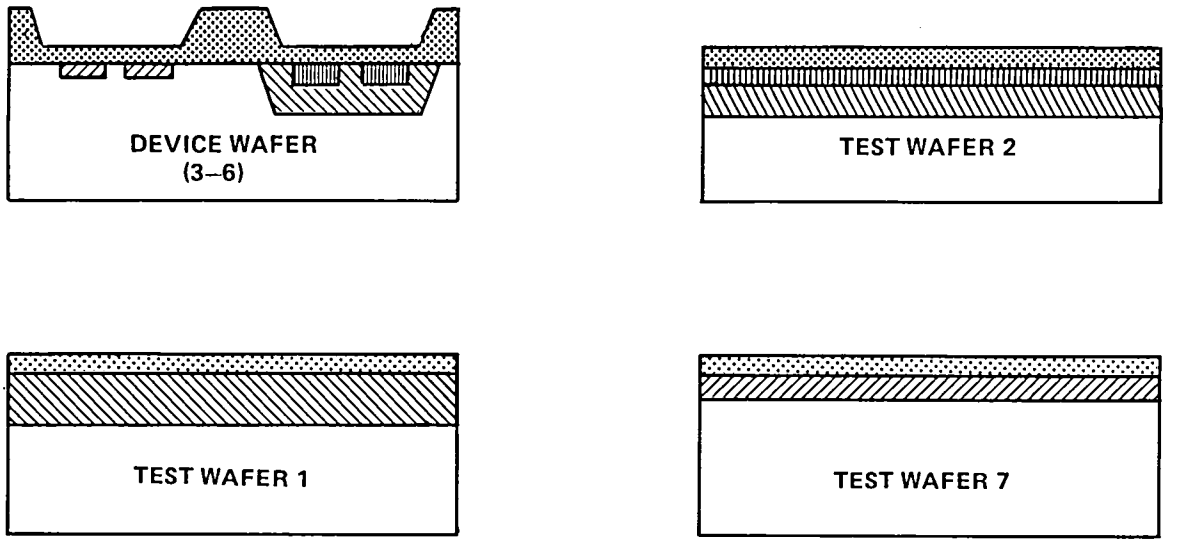


Figure 23. Gate oxidation.

5. Gate anneal 1423°K (1150°C) 50 mm tube
(1-7, 1(P-/N-), 2(N+/P-/N-), 7(P+/N-) gate oxide)

   a. N_2 31 cm^3/s 900 s (15 min)

H. CONTACT ETCH

1. PR with Mask 5
(3-6)

   a. Apply PR
   b. Spin at 100 rps 15 s
   c. Prebake in N_2 at 333°K (60°C) 1800 s (30 min)
   d. Align Mask 5
   e. Expose with UV light 12 mJ/cm^2 t = (2-4) s
   f. Spray develop with PR developer 15 s
   g. Spray rinse with PR rinse 15 s
   h. Spin dry at 100 rps 15 s
   i. Postbake in N_2 at 413°K (140°C) 1800 s (30 min)

2. Contact etch (Fig. 24)
(1-7, 1(P-/N-), 2(N+/P-/N-), 7(P+/N-) gate oxide)

   a. Etch #2, 7, 1 in BOE at RT t = (60-80) s
   b. Etch #3-6 in BOE at RT t+15 s
   c. Rinse in H_2O 600 s (10 min)

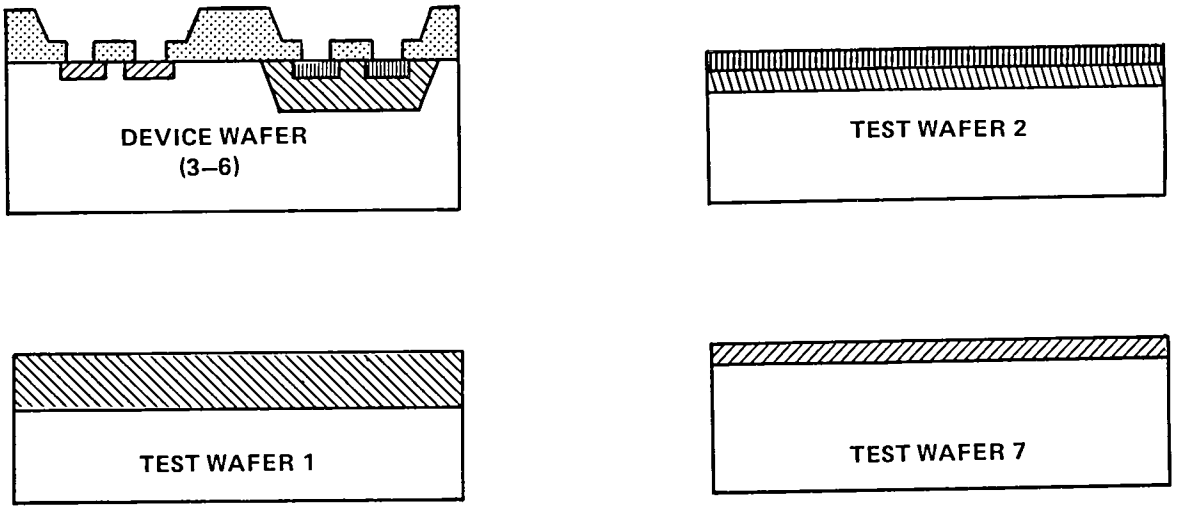


Figure 24. Metal contact cutouts and gate thickness definition.

3. PR strip
(3-6)

a. Strip PR in SP solution (freshly mixed) 300 s (5 min)
b. Rinse in H_2O 600 s (10 min)

4. Final resistivity check
(1(P-/N-) 2000-2200 Ω /□, 2(N+/P-/N-) 15-25 Ω /□, 7(P+/N-) 80-150 Ω/□)

a. Measure R_s of #1

1: _____ 2: _____ 3: (2000-2200) 4: _____ 5: _____

b. Measure R_s of #2

1: _____ 2: _____ 3: (15-20) 4: _____ 5: _____

c. Measure R_s of #7

1: _____ 2: _____ 3: (80-120) 4: _____ 5: _____

I. FIRST METALLIZATION

1. Pre-metal clean
(3-6)

a. Etch #3-6 in HF solution at RT (freshly mixed) 60 s (1 min)
b. Rinse in H_2O 600 s (10 min)
c. Blow dry with N_2

2. Dehydration (3-6) 1173°K (900°C) 50 mm tube

a. N_2 31 cm^3/s 600 s (10 min)

3. Metallization (3-6) 0.5 μm (Fig. 25) 700 mPa (5 μm Hg)

a. Magnetron sputter deposit 6061 Al alloy in argon with 120 s (2 min) shutter time at 3 A, 450 V 720 s (12 min)

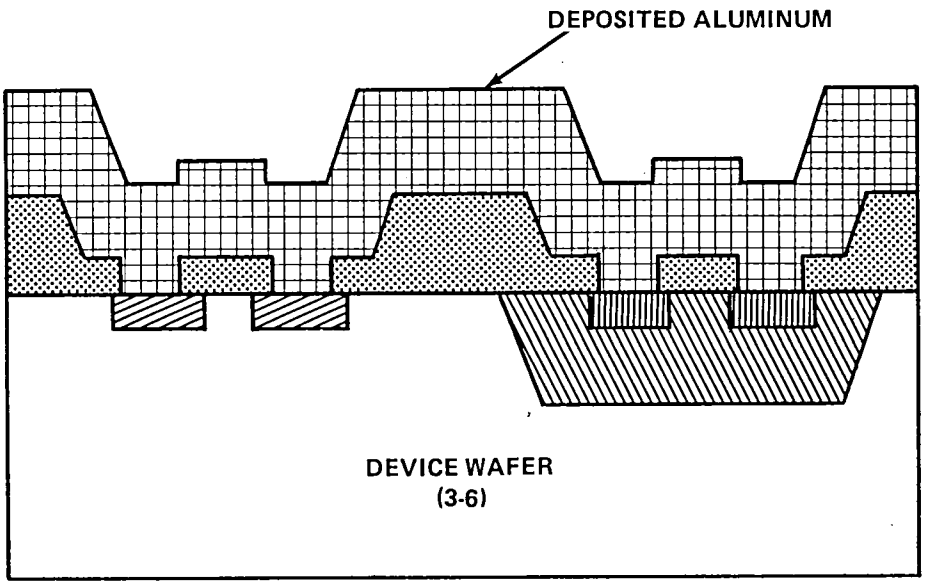


Figure 25. Metal deposition.

4. PR with Mask 6 (3-6, first metal)

a. Apply PR
b. Spin at 100 rps 15 s
c. Prebake in N_2 at 333°K (60°C) 1800 s (30 min)
d. Align Mask 6
e. Expose with UV light 9 mJ/cm^2 t = (1.5-3) s
f. Spray develop with PR developer 15 s

g. Spray rinse with PR rinse — 15 s
h. Spin dry at 100 rps — 15 s
i. Postbake in N_2 at 413°K (140°C) — 1800 s (30 min)

5. Metal etch (Fig. 26)
(3-6, first metal)

a. Etch #3-6 in Al etch at 313°K (40°C) — $t = \frac{(60-75)}{600\text{ s (10 min)}}$ s
b. Rinse in H_2O

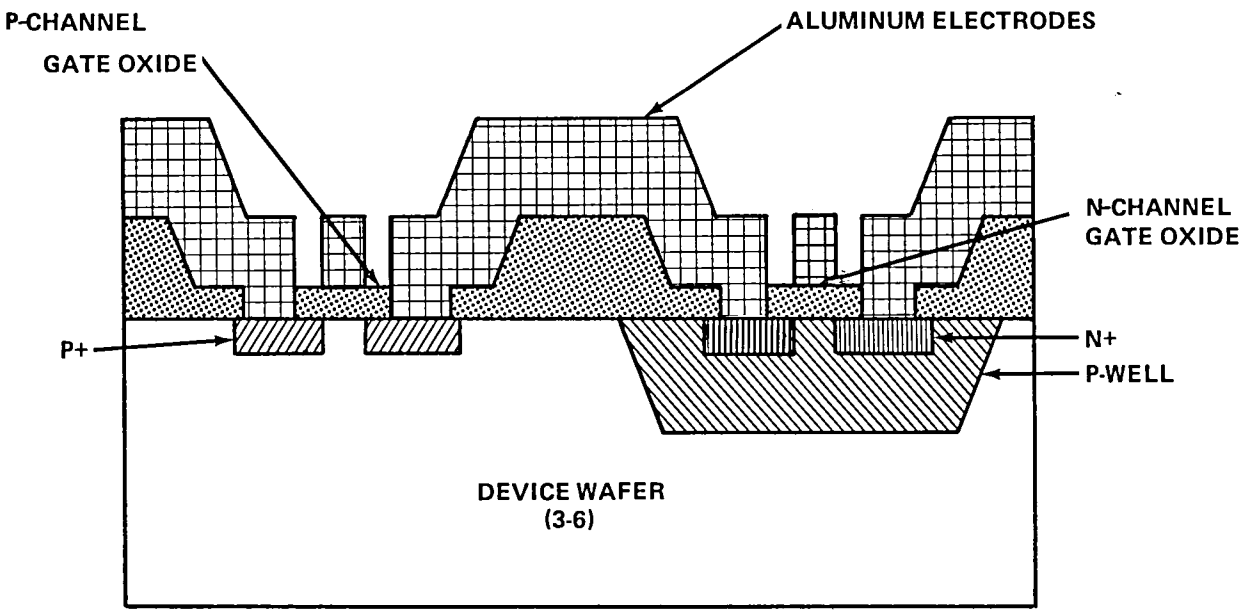


Figure 26. Metal etch.

6. PR strip
(3-6, first metal)

a. Strip PR in SCr solution at RT — 1800 s (30 min)
b. Rinse in H_2O — 600 s (10 min)
c. Blow dry with N_2

J. INTERMETAL OXIDE

1. Intermetal oxide — 800 nm (Fig. 27) — 673°K (400°C) Silox CVD
(2-6, 2(N+/P-/N-) no oxide)

a. N_2	320 cm^3/s 300 s (5 min)
b. N_2	320 cm^3/s
O_2	5.3 cm^3/s
SiH_4 (4% in Ar)	6.4 cm^3/s t = $\frac{(1200-1500)}{}$ s
c. N_2	320 cm^3/s 600 s (10 min)

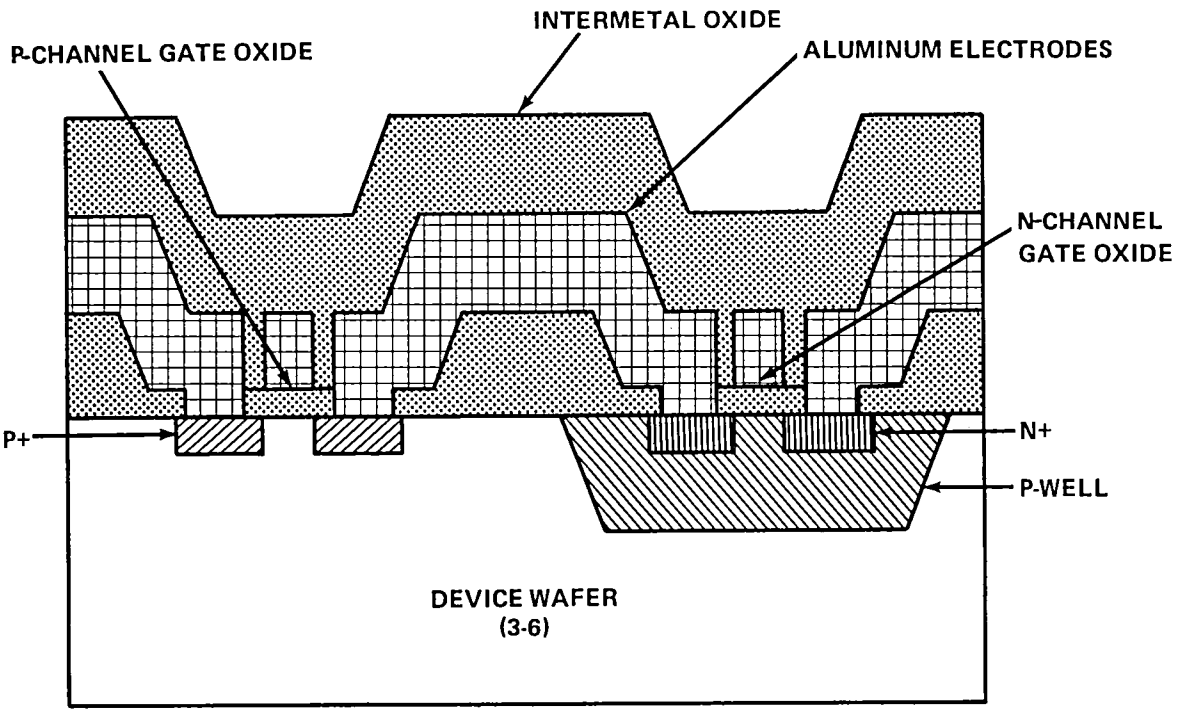


Figure 27. Intermetal oxide.

2. PR with Mask 7
(3-6, intermetal oxide)

a. Apply PR	
b. Spin at 100 rps	15 s
c. Prebake in N_2 at 333°K (60°C)	1800 s (30 min)
d. Align Mask 7	
e. Expose with UV light 6 mJ/cm^2	t = $\frac{(1-2)}{}$ s
f. Spray develop with PR developer	15 s
g. Spray rinse with PR rinse	15 s
h. Spin dry at 100 rps	15 s
i. Postbake in N_2 at 413°K (140°C)	1800 s (30 min)

3. Via etch (Fig. 28)
(2-6, 2(N+/P-/N-) intermetal oxide)

a. Etch #2 in BOE etch at RT	$t = \frac{(120\text{-}180)}{t+60\ s}$ s
b. Etch #3-6 in BOE etch at RT	
c. Rinse in H_2O	600 s (10 min)

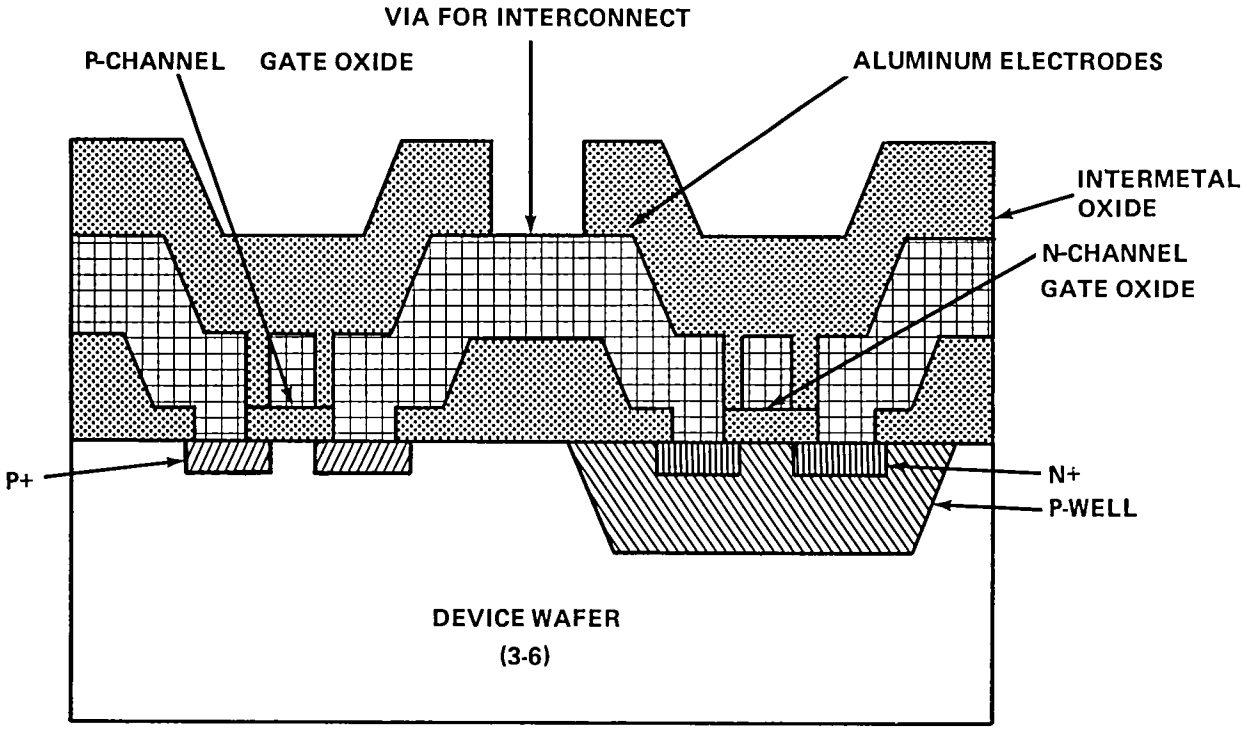


Figure 28. Intermetal oxide cutout.

4. PR strip
(3-6, intermetal oxide)

a. Strip PR in SCr solution at RT	1800 s (30 min)
b. Rinse in H_2O	600 s (10 min)
c. Blow dry with N_2	

K. SECOND METALLIZATION

1. Metallization (3-6)	0.5 μm (Fig. 29)	700 mPa (5 μm Hg)

a. Magnetron sputter deposit 6061 Al alloy in argon with 120 s (2 min) shutter time at 3 A, 450 V — 720 s (12 min)

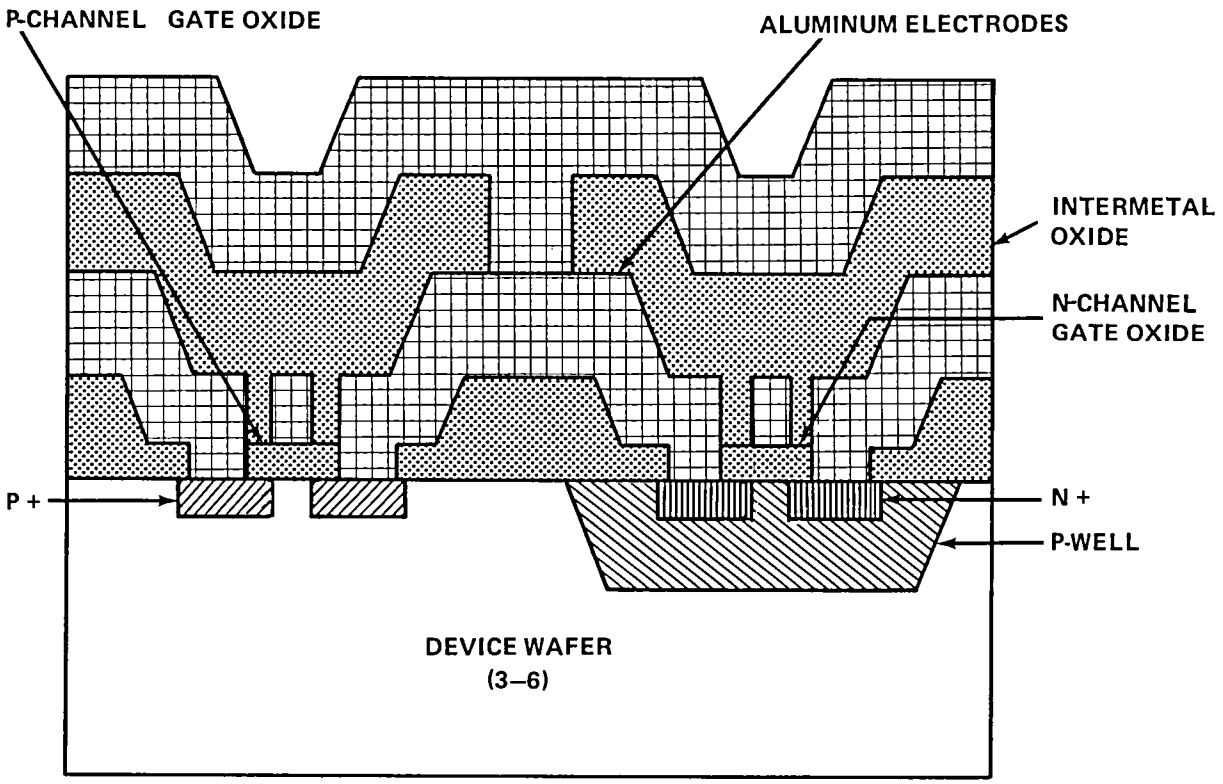


Figure 29. Second level metallization.

2. PR with Mask 8
(3-6, second metal)

a. Apply PR	
b. Spin at 100 rps	15 s
c. Prebake in N_2 at 333°K (60°C)	1800 s (30 min)
d. Align Mask 8	
e. Expose with UV light 9 mJ/cm^2	t = (1.5-3) s
f. Spray develop with PR developer	15 s
g. Spray rinse with PR rinse	15 s
h. Spin dry at 100 rps	15 s
i. Postbake in N_2 at 413°K (140°C)	1800 s (30 min)

3. Metal etch (Fig. 30)
(3-6, second metal)

a. Etch #3-6 in Al etch at 313°K (40°C) t = (60-75) s
b. Rinse in H_2O 600 s (10 min)

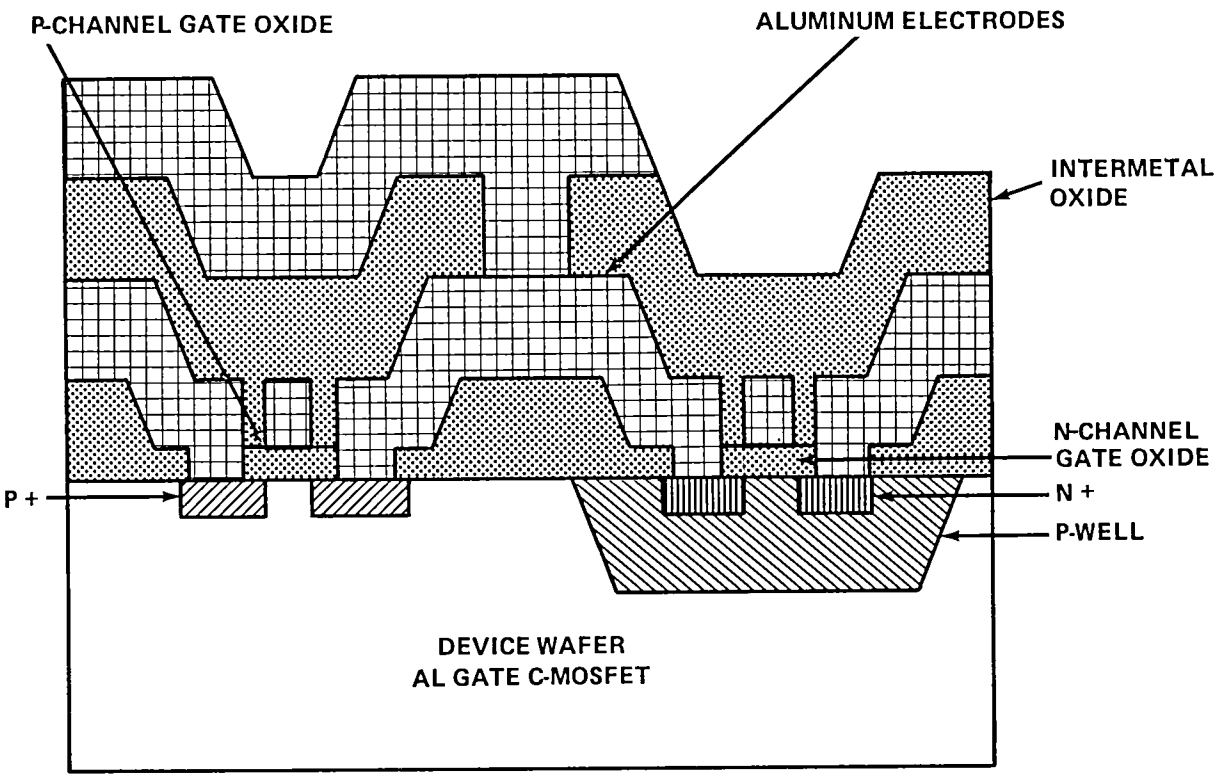


Figure 30. Second level metal definition.

4. PR strip
(3-6, second metal)

a. Strip PR in SCr solution at RT 1800 s (30 min)
b. Rinse in H_2O 600 s (10 min)
c. Blow dry with N_2

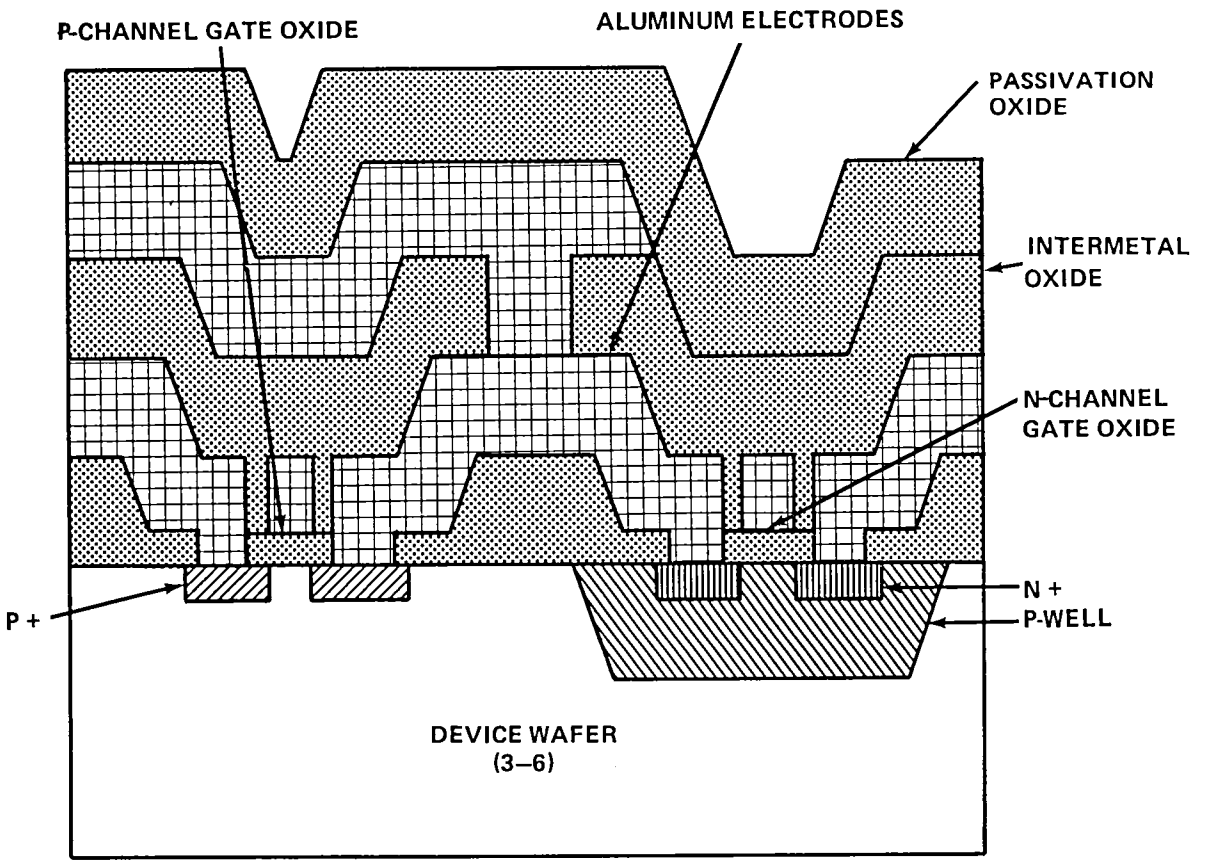
5. Sinter second metal 743°K (470°C) 74 mm tube
(3-6, second metal)

a. N_2 40 cm^3/s 900 s (15 min)

L. PASSIVATION

1. Passivation oxide 800 nm (Fig. 31) 673°K (400°C) Silox CVD
(2-6, 2(N+/P-/N-) no oxide)

a. N_2	320 cm^3/s 300 s (5 min)
b. N_2	320 cm^3/s
O_2	5.3 cm^3/s
SiH_4 (4% in Ar)	6.4 cm^3/s t = (1200-1500) s
c. N_2	320 cm^3/s 600 s (10 min)



COMPLETED
AL GATE C-MOSFET
DOUBLE LEVEL METALLIZATION

Figure 31. Passivation.

2. PR with Mask 9
(3-6, passivation oxide)

a. Apply PR	
b. Spin at 100 rps	15 s
c. Prebake in N_2 at 333°K (60°C)	1800 s (30 min)

d. Align Mask 9
e. Expose with UV light 6 mJ/cm^2 — t = (1-2) s
f. Spray develop with PR developer — 15 s
g. Spray rinse with PR rinse — 15 s
h. Spin dry at 100 rps — 15 s
i. Postbake in N_2 at 413°K (140°C) — 1800 s (30 min)

3. Passivation oxide etch
(2-6, 2(N+/P-/N-) intermetal oxide)

a. Etch #2 in BOE etch at RT — t = (120-180) s
b. Etch #3-6 in BOE etch at RT — t+15 s
c. Rinse in H_2O — 600 s (10 min)

4. PR strip
(3-6, passivation oxide)

a. Strip PR in SCr solution at RT — 1800 s (30 min)
b. Rinse in H_2O — 600 s (10 min)
c. Blow dry with N_2

M. ELECTRICAL TEST PARAMETERS

____ 1st _x_ 2nd Metal Testing: _____ Drop-in _x_ On-chip

Transistor Parameters

W_P = (50) μm W_N = (50) μm

L_P = (7.5) μm L_N = (7.5) μm

		Wafer #3		Wafer #4		Wafer #5		Wafer # 6	
		P	N	P	N	P	N	P	N
	1:								
	2:								
V_T(V)	3:	(-1.5)	(1.4)	(-2.0)	(1.8)				
	4:								
	5:								

		Wafer #3		Wafer #4		Wafer #5		Wafer #6	
		P	N	P	N	P	N	P	N
	1:								
	2:								
BV_{DSS} (V)	3:	(-30)	(25)	(-32)	(28)				
	4:								
	5:								
	1:								
	2:								
g_m (μS)	3:	(280)	(420)	(320)	(460)				
	4:								
	5:								
	1:								
	2:								
Beta (A/V^2)	3:	$(2(10^{-4}))$	$(-2(10^{-4}))$	$(5(10^{-4}))$	$(-5(10^{-4}))$				
	4:								
	5:								
	1:								
	2:								
I_{DSS} (nA)	3:	(-1)	(1)	(-2)	(2)				
	4:								
	5:								
	1:								
	2:								
BV_{GSS} (V)	3:	(-80)	(80)	(-100)	(100)				
	4:								
	5:								

Test Conditions

V_T : V_{GS} = 10 V, I_{DS} = 10 μA

BV_{DSS} : V_{GS} = 0 V, I_{DS} = 1 μA

g_m : V_{DS} = 10 V, I_{DS} = 1 mA

I_{DSS} : V_{DS} = 10 V, V_{GS} = 0 V

BV_{GSS} : V_{DS} = 0 V, I_{GS} = 1 μA

Functional Test Yield _____ %

N. PROCESS TEST PARAMETERS

Wafer # _____ Testing: C017 Drop-in _____ On-chip

Sheet Resistance

P+	P-	N+
1: _____	1: _____	1: _____
2: _____	2: _____	2: _____
3: (80-120)	3: (2000-2200)	3: (15-20)
4: _____	4: _____	4: _____
5: _____	5: _____	5: _____

Metallization Integrity

Via Continuity	Second Metal Continuity	Intermetal Continuity
1: _____	1: _____	1: _____
2: _____	2: _____	2: _____
3: _____	3: _____	3: _____
4: _____	4: _____	4: _____
5: _____	5: _____	5: _____

C-V Analysis

V_{FB} at RT (V)

	P	N
1:	_____	_____
2:	_____	_____
3:	(-0.6 to -0.8)	(-0.8 to -1.1)
4:	_____	_____
5:	_____	_____

Q_{ss} (#/cm^2)

	P	N
1:	_____	_____
2:	_____	_____
3:	(5-8 (10^{10}))	(5-8 (10^{10}))
4:	_____	_____
5:	_____	_____

V_{FB} shift at RT (V)

1:	_____	_____
2:	_____	_____
3:	(0 to -0.1)	(0 to -0.1)
4:	_____	_____
5:	_____	_____

V_{FB} shift after T&B (V)

1:	_____	_____
2:	_____	_____
3:	(-0.2 to -0.5)	(-0.2 to -0.5)
4:	_____	_____
5:	_____	_____

V. EXPLANATION OF C-MOS PROCESS

An explanation of the concepts of and the reasons for the various segments of the MSFC process are presented as an aid to understanding this C-MOS effort. A brief description of the facility requirements is provided. The two ambients, room environment and water, to which the wafer is primarily exposed during processing are critical to the electrical parameters and processing yields of C-MOS IC's.

A. Water

The water used in the processing of C-MOS IC's is required to be extremely free of contaminants and to exhibit an extremely high resistivity. The production of the water for use in all processing steps at MSFC begins with a high pressure steam source. Steam from this source is sent through a heat exchanger to condense the steam into water which has approximately 3 ppm total dissolved solids (tds) content. The water then passes through a 3-μm filter and enters a two-bed (cation-anion) demineralizer where the water leaving has approximately 1/2 ppm tds and 3 Mohm resistivity. A mixed-bed (cation-anion) deionizer is then used to obtain water with approximately 1.4 ppm tds and 18 Mohm resistivity. Filtered through a 1-μm filter, the water enters another mixed-bed deionizer which supplies water to the processing laboratory with an extremely low particulate count and an extremely high resistivity.

B. Cleanroom

Processing of C-MOS IC's must be performed in a cleanroom environment [8]. In a cleanroom the internal air pressure is positive with respect to the exterior air pressure so that air leaks in the facility will not contaminate the interior. The air is completely exchanged frequently with clean filtered air. The temperature and humidity are controlled to approximately 294°K (21°C) and 45 percent, respectively.

C. Wafers

Silicon wafers used in the MSFC fabrication facility are typically 38 mm (1.5 in.) in diameter and from 0.25 to 0.30 mm (10 to 12 mils) thick. One side of the wafer (active side) is mechanically and chemically polished while

the other side is chemically etched to relieve stresses. The bulk material used for this C-MOS process is <100> orientation single crystal silicon. Each wafer has a <110> orientation flat to which the IC patterns are prealigned parallel and perpendicular to the crystal planes. This alignment allows the IC's to be separated accurately. All wafers are doped N-type with phosphorus ions to a concentration of approximately 1×10^{15} ions/cc and have a resistivity between 3 and 6 ohm-cm. Wafers to the previously given specifications may be ordered from silicon wafer manufacturers.

D. P-Well Masking Oxide

The first procedure is to clean the wafers and prepare them for the P-well masking oxide to be grown. The wafers are placed on a spinner where they are sprayed with ethyl alcohol. While being sprayed, they are scrubbed with a nylon bristle brush. They are then spun dry. This is the alcohol brush spin (ABS) cleaning procedure.

The wafers are now prepared for oxidation by loading them into a quartz carrier called a "boat" and placing them into a quartz tube in an accurately controlled, high temperature cylindrical furnace. Accurately controlled flows of high purity gases from liquid or gas sources are injected into the furnace tube. Oxygen reacts with the silicon to produce silicon dioxide on the surfaces of the wafers. The oxygen atoms diffuse through the existing oxide layer to the silicon-silicon dioxide interface where the oxidation occurs. Steam is used to increase the rate at which the reaction occurs. Curves for growth rate of silicon dioxide on silicon according to orientation, temperature, and atmosphere are provided in Appendix B. The steam is produced by boiling DI water. Dry oxygen is again used to produce a high quality silicon dioxide layer at the interface between the silicon dioxide and the silicon. At the end of the oxidation sequence, nitrogen is used to anneal the silicon dioxide by allowing the remaining uncombined atoms of oxygen trapped in the silicon dioxide to react with the silicon. The P-well masking oxide is used to protect the silicon in which a P-well is not to be formed.

The wafers, immediately from the furnace, are placed on a rapid acceleration spinner where they are held on a chuck by a vacuum. Negative type photoresist (PR), a light sensitive liquid plastic polymer, is applied to the surface of the wafer from a dropper bottle. The wafer is rapidly accelerated creating a thin coating of uniform thickness while the excess is removed by "centrifugal" force. The coated wafers are then prebaked in an oven (purged by nitrogen) to remove excess solvents and promote adhesion. Using mask 1, which

has opaque and clear patterns, a mask aligner is used to align the mask to the wafer within a 1/2 μ tolerance. The mask aligner is equipped with a split-field microscope which enables the operator to view both sides, left and right, of the wafer simultaneously during alignment. The wafers are then exposed through the mask with high intensity ultraviolet light using negative type PR. The PR under the clear regions of the mask is polimerized during exposure, while the other PR remains unpolimerized. This photographic process is commonly termed, in the microelectronics industry, photolithography.

The unexposed photoresist is removed by spray developing and rinsing using suitable solvents. The exposed photoresist, which was under the clear areas of the mask, remains to protect the oxide during oxide etching to define the necessary pattern. The wafers are then postbaked to remove most of the remaining solvents, to harden the photoresist, and to ensure adhesion of the photoresist to the wafer surface. They are now placed into a solution of buffered oxide etchant (BOE) so that cutouts may be etched for the boron P-well. The BOE etches away the unprotected silicon dioxide but does not rapidly attack the silicon underneath. After the etch is completed, rinsing the wafers in DI water removes the excess etching solution remaining on the surface. Since the photoresist is no longer needed, it is removed in the SP solution. This solution is rinsed away with water and the wafers are blown dry with nitrogen.

E. P-Well Implantation or Diffusion

Two methods of creating a P-well are by ion implantation and by diffusion. Both methods have been used at MSFC, but ion implantation is preferred because it requires less time and provides a P-well of more uniform resistivity from wafer to wafer. However, both methods will be discussed.

Ion implantation is used to introduce a precisely controlled number of P-type boron dopant ions into the exposed silicon surface, i.e., that portion of the wafer which is not protected by the P-well masking oxide. The number of ions implanted is controlled by the ion beam current and the implantation time, and the depth of the implant is controlled by the acceleration voltage. The implantation is made through a thin thermal oxide to protect the silicon surface from the direct bombardment of the ion beam. This thin oxide, together with the P-well masking oxide, is removed in BOE prior to the drive-in. The implanted ions are then diffused into the silicon to the required depth in a high temperature furnace while a layer of silicon dioxide is grown to prevent the outgassing of the dopant, to deplete the dopant, and to form a masking oxide for later diffusions. Virtually all of the implanted ions which are diffused into the

silicon become electrically active during the diffusion. Therefore, the accuracy of the doping concentration is limited only by the accuracy of the measurement made by the ion dosage integrator during the implantation process.

The second method of creating a P-well is by diffusion and does not require a thin oxide to protect the silicon surface. This technique utilizes boron nitride (BN) wafers as dopant sources. The BN diffusion boat has slots in which the silicon wafers are placed a fixed distance from the surface of the BN wafers. Before a diffusion, the BN wafers must be oxidized to form boron oxide (B_2O_3) on their surface. This B_2O_3 is the diffusion source for the P-well diffusion. For a diffusion the boat is placed into a high temperature furnace where the B_2O_3 on the BN wafers act as a source of boron ions which diffuse into the unprotected silicon windows. A curve for the diffusion of BN is provided in Appendix C. Nitrogen is used as the ambient gas to prevent the growth of an oxide on the silicon which will prevent the diffusion. Some borosilicate glass is grown, however, from the B_2O_3 and must be completely removed. The BOE will remove most, but not all, of this oxide. Jacobson's etchant is used to soften the remaining very thin, heavily boron doped glass so it can be etched away by the BOE. The boron diffusion at this point is too highly concentrated for the P-well and therefore some of the dopant ions must be removed. Boron lends itself nicely to depletion during subsequent oxidations due to its segregation coefficient. By carefully controlling the temperature of the furnace and the ambient used, the proper amount of boron ions will be removed (entering the oxide and later removed) and the remaining ions, when diffused into the silicon to a specified depth, will give the correct dopant concentration for the P-well. This procedure is more involved and time consuming when compared with the ion implantation procedure, but trying to initially dope the P-well lightly with diffusion techniques generally yields nonuniform and nonreproducible results.

F. P+ Diffusion

The photolithographic process is repeated using mask 2 to define the areas where the P+ boron diffusion will take place. After the wafers are etched, the photoresist is removed by the procedure previously given. The P+ diffusion to form the source and drain regions of the P-MOS devices is similar to the procedure given for the diffusion technique for obtaining a P-well. However, no oxidations are used to deplete the boron concentration from the silicon surface.

G. Diffusion Resistivity Measurements

It is desirable to know the impurity concentration of the device wafer after each diffusion or ion implantation step in the process. Therefore, after removal of all protective oxides a resistivity measurement is made on a sample wafer to determine the impurity concentration of that sample. Because the sample and device wafers were subjected to the same diffusion (or ion implantation) conditions, the measured concentration of the sample wafer is taken to be the doping level of the device wafer. The number of dopant ions present in the wafer lattice directly affects the number of free electrons in the conduction band and therefore the ability of the material to conduct current. The resistivity readings therefore can be related directly to the doping level. These readings are taken on the surface of the wafer and knowing the junction depth and assuming a gaussian profile provide a good approximation to the concentration of the dopant material.

H. N+ Diffusion Masking Oxide

After the borosilicate glass (grown during the P+ boron diffusion) has been softened and etched away, a thermal oxide is grown in a high temperature furnace to act as a masking oxide during the N+ diffusion and to help remove any residual borosilicate glass. The oxidation procedure is similar to the one previously described in Paragraph D (P-Well Masking Oxide).

I. N+ Diffusion

The photolithographic process is repeated using mask 3 to define the areas where the N+ phosphorus diffusion will take place. After the wafers are etched, the photoresist is removed by the procedure previously given. The wafers are then placed in a high temperature furnace where the N+ diffusion occurs, which forms the source and drain regions of the N-MOS devices.

J. Field Oxide

At this step in the process, all of the oxides of various thicknesses are removed by etching with BOE. This "etch back" process allows the growth of clean high quality field oxide that will be generally of uniform thickness and exhibit a uniform etch rate. The thermal oxide, which has a maximum thickness of 400 nm over the N+ regions, is grown over the entire wafer.

K. Gate Oxide

The photolithographic process is repeated using mask 4 to define the areas where the gate oxide is to be grown. After the wafers are etched, the photoresist is removed by the process previously given. They are rinsed, blown dry, and placed in a high temperature furnace where the gate oxide is grown. The furnace oxidizing atmosphere is a HCl-steam vapor produced by boiling an azeotropic mixture of hydrochloric acid and water. This mixture allows the use of a lower temperature furnace than could be used with dry oxygen and also provides a gettering action against mobile ion contamination. An excess amount (10 to 15 percent) of gate oxide is grown which will be removed later. This excess is removed because most of the mobile ion contamination is in the top 10 to 15 percent of the oxide.

L. Metal Contacts

The photolithographic process is repeated using mask 5 to define the areas in which the metal will make contact to the diffusions. Mask 5 is aligned to the pattern on the wafer. After the wafers are etched, the photoresist is removed by the procedure previously given but omitting the drying step and proceeding into the premetal clean. The wafers are etched during the premetal clean to obtain a final gate oxide thickness between 100 and 105 nm.

M. Metallization

The wafers are cleaned immediately before deposition of metal which will become the metal lines and bonding pads to interconnect the circuit. A direct current, low power, hollow cathode sputtering system is used to deposit the metal. This system is operated at 2-3 A and 350-450 V. The wafers are placed on a rotating platform and the system is placed under a vacuum of 700 μPa (5 nm of Hg). The pressure is then raised to 700 mPa (5 μm of Hg) by a controlled leak of argon gas. After shuttering the wafers from the deposition source for 2 min, target metal is sputtered onto the wafers. Immediately after removal from the metallization system, the wafers go through the photolithographic process again using mask 6 which is aligned to the pattern on the wafer. The wafers are then etched in metal etchant to define the metal interconnect lines in the circuits. After a water rinse, the photoresist is removed in a bath of metal-compatible photoresist remover which does not significantly attack the metal. The wafers are then given a final blow dry with N_2.

In the case of aluminum metallization, if two (or more) levels of metal interconnects are to be used then care must be taken to eliminate or reduce the generation of hillocks (caused by electromigration) on the first level of metallization. The growth of hillocks on the first level of metallization will increase the possibility of subsequent metal levels shorting to the first level metal due to the hillock protruding through the insulation oxide. Hillock growth can be reduced by using aluminum alloys such as 96 percent Al, 4 percent Cu, and others.

N. Intermetal Oxide

The wafers are loaded into a chemical vapor deposition (CVD) system. The temperature is raised and allowed to stabilize. Oxygen and silane (4 percent silane in argon) are injected into the system simultaneously and thermally decomposed to form silicon dioxide which is deposited onto the surface of the wafers. The system is allowed to cool and the wafers are removed. The wafers are immediately coated with photoresist and go through the photolithographic process using mask 7 which is aligned to the pattern on the wafer. BOE is used to etch the silicon dioxide from the bonding pads and vias. The photoresist is removed using the metal-compatible photoresist remover.

Care must be taken to avoid overexposure if multilevel metal is being used. Since the metal on the wafer reflects much more light than any of the oxides of silicon, the exposure time may need to be reduced. Rounded and undersized vias for the interconnect may result otherwise.

O. Second Metallization

The wafers are rinsed thoroughly with DI water after stripping the photoresist with a metal-compatible photoresist stripper. Then the sputtering process used for the first metal is used to deposit the second metal. Afterwards a photoresist procedure, as in Paragraph M, is used with mask 8. The metal levels are then sintered to the silicon wafer and to each other in a low temperature furnace where a nitrogen ambient is used to prevent the growth of metal oxides. This sintering procedure not only reduces the series resistance between the metals and the metals and the silicon wafer, but also removes most of the charges introduced during the sputtering process.

P. Passivation

The wafers are again loaded into the CVD system after stripping the photoresist and rinsing with DI water. The oxide deposition masking, etching, and stripping procedure of Paragraph N is repeated using mask 9. This is the final step of double level metallization process.

Q. Metal Level Variations

For more than two levels of metal interconnects, Paragraphs O and P are repeated as necessary using subsequent mask levels. In each case, sintering, as described in Paragraph O, is performed only after the last metal level has been deposited. In the case of a single level metallization process, the sintering is performed after the first level metal deposition.

VI. CONCLUDING REMARKS

A. C-MOS Process

The C-MOS process described in this report has been used successfully at MSFC to produce IC's which have been functioning reliably in active systems. Since this C-MOS process has been proven successful at MSFC, it can therefore be utilized by industry, universities, other NASA centers, and other agencies of the Government in the production of C-MOS IC's. The process is given in detail to aid in its utilization, while the explanation is given to aid those unfamiliar with IC processing toward a general understanding of how and why certain steps are performed. A detailed explanation of all phases of processing is not within the scope of this report since many books and papers have been written on these subjects.

B. MSFC Facility

The brief description of the IC facility at MSFC, given to demonstrate an overall view of the requirements of IC production, shows the capabilities in microelectronics which MSFC has in-house. This facility has the capability of producing many types of IC's other than C-MOS while serving three important functions for NASA.

1. Research and Development. Much research and development work is performed in the Electronics Development Division of MSFC. Technology development at the state-of-the-art level of MOS microelectronics is accomplished by in-house innovation and following closely the trends of the industry. The establishment and verification of new processes or processing methods are major tasks of this division. In some cases, new technologies are developed and verified which are then provided to industry to establish new and improved products.

2. Education. The training of personnel in NASA, other agencies of Government, industry, and universities is another major function that is performed. Many personnel in NASA and other governmental agencies have been trained in microelectronics technology so that they can establish requirements for industries which supply microcircuits for their applications. Industries providing devices for NASA applications are required to have their processing facilities certified by NASA. Other NASA personnel have received training when such training proved useful in their scope of work. Much written information has been provided to other NASA centers, governmental agencies, universities, and industries in addition to training. Tours and informal conferences are often held for the benefit of industry personnel or for university professors and students who have a need or desire for information concerning microelectronics. Research contracts with industries and universities provide another means of increasing the state of the technology.

3. Circuits. In experiments or direct NASA applications, small quantities of research and developmental circuits (which are not needed in sufficient quantities to make them commercially feasible) are produced. These circuits are specifically designed to meet the user's exact requirements to fulfill a necessary function. Custom circuits, necessary for the support and completion of university research contracts and technology performance studies, have been produced. Specialized circuits have been produced for university professors on special assignment with NASA for experiments on the physics of semiconductor devices. In the future, many types of research and development circuits needed by NASA can be produced to fulfill program goals. These capabilities are the culmination of a total effort in the Electronics Development Division to possess the required technology to produce IC's from conceptual design through final testing.

George C. Marshall Space Flight Center
National Aeronautics and Space Administration
Marshall Space Flight Center, Alabama 35812, July 1978

APPENDIX A

CHEMICAL SOLUTIONS USED IN C-MOS PROCESS

Several chemical solutions used in the processing of C-MOS IC must be mixed by the processor. Some of these solutions cannot be readily found in the mixed form while others should be mixed immediately before use. All chemicals used in processing should be reagent grade, electronic grade, or equivalent to prevent contamination of the wafers. Values in parentheses denote concentration of chemicals used.

	SCr — Sulfuric-Chromic Stripper	
55 g	H_2SO_4	Sulfuric Acid (98%)
1 g	CrO_3	Chromic Acid Anhydride — Crystal (Chromium Trioxide)
	Aluminum Etchant	
25 cc	H_3PO_4	Phosphoric Acid (85%)
5 cc	CH_3COOH	Acetic Acid-Glacial (100%)
1 cc	HNO_3	Nitric Acid (70%)
	BOE — Buffered Oxide Etchant	
5 g	NH_4F	Ammonium Flouride — Crystal
2 cc	HF	Hydroflouric Acid (49%)
8 cc	H_2O	Water (18 MΩ)
	Hydroflouric Acid Solution	
1 cc	HF	Hydroflouric Acid (49%)
10 cc	H_2O	Water (18 MΩ)

Jacobson's Etchant

25 cc	H_2O	Water (18 MΩ)
5 cc	HCl	Hydrochloric Acid (37%)
5 cc	HNO_3	Nitric Acid (70%)
1 cc	H_2SO_4	Sulfuric Acid (98%)

SP — Sulfuric Hydrogen Peroxide Stripper

2 cc	H_2SO_4	Sulfuric Acid (98%)
1 cc	H_2O_2	Hydrogen Peroxide (30%)

$HCl:H_2O$ Azeothropic Solution

103 cc	HCl	Hydrochloric Acid (37%)
100 cc	H_2O	Water (18 MΩ)

APPENDIX B

SILICON DIOXIDE GROWTH RATES

Silicon dioxide growth rates vary according to several factors, the most important being silicon crystal orientation, atmosphere, time, and temperature. The silicon wafers used in the C-MOS process have <100> orientation. Silicon exposed to a steam atmosphere will oxidize faster than silicon in dry oxygen. Silicon dioxide will increase in thickness when exposed for longer periods of time, and the growth rate increases as the temperature of the reaction is increased. The graphs [9] are of oxide thickness versus time for various temperatures on <100> orientation silicon wafers in the given atmosphere (Figs. B-1 and B-2).

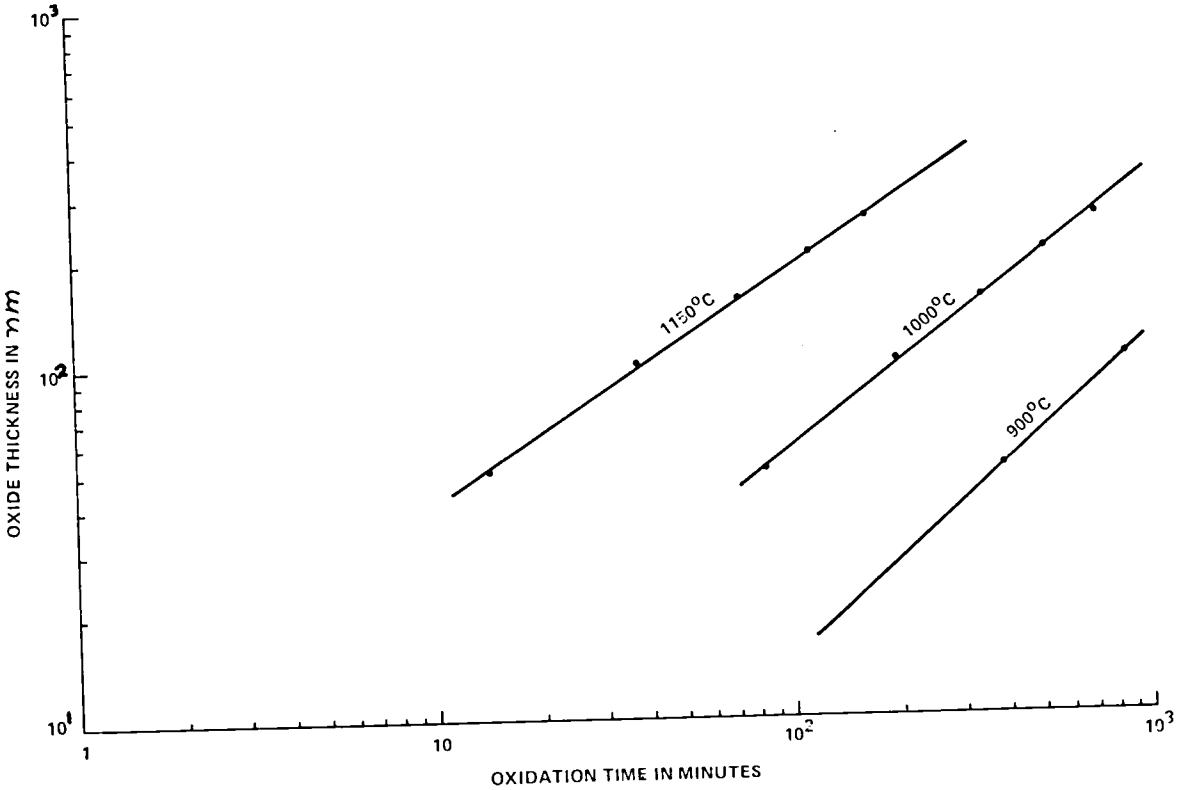


Figure B-1. <100> Si, SiO_2 growth rate curves in dry O_2.

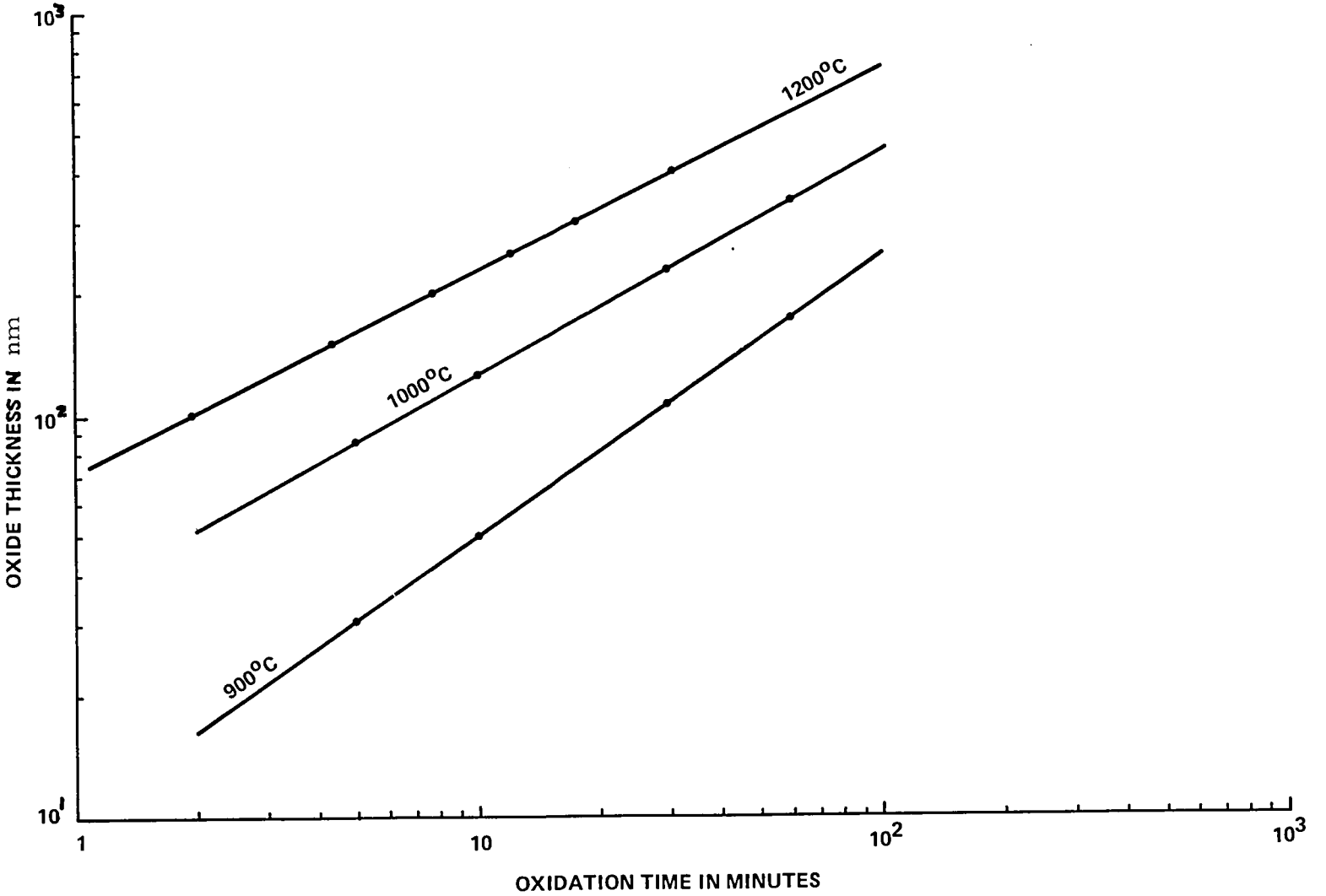


Figure B-2. <100> Si, SiO_2 growth rate curves in stream.

APPENDIX C

BORON NITRIDE DIFFUSIONS

Boron nitride (grade A) diffusions are primarily dependent upon time and temperature. Figure C-1 presents sheet resistivity versus deposition time at various temperatures. Sheet resistance is defined in units of ohms per square unit of area (□) because it is a function of geometry.

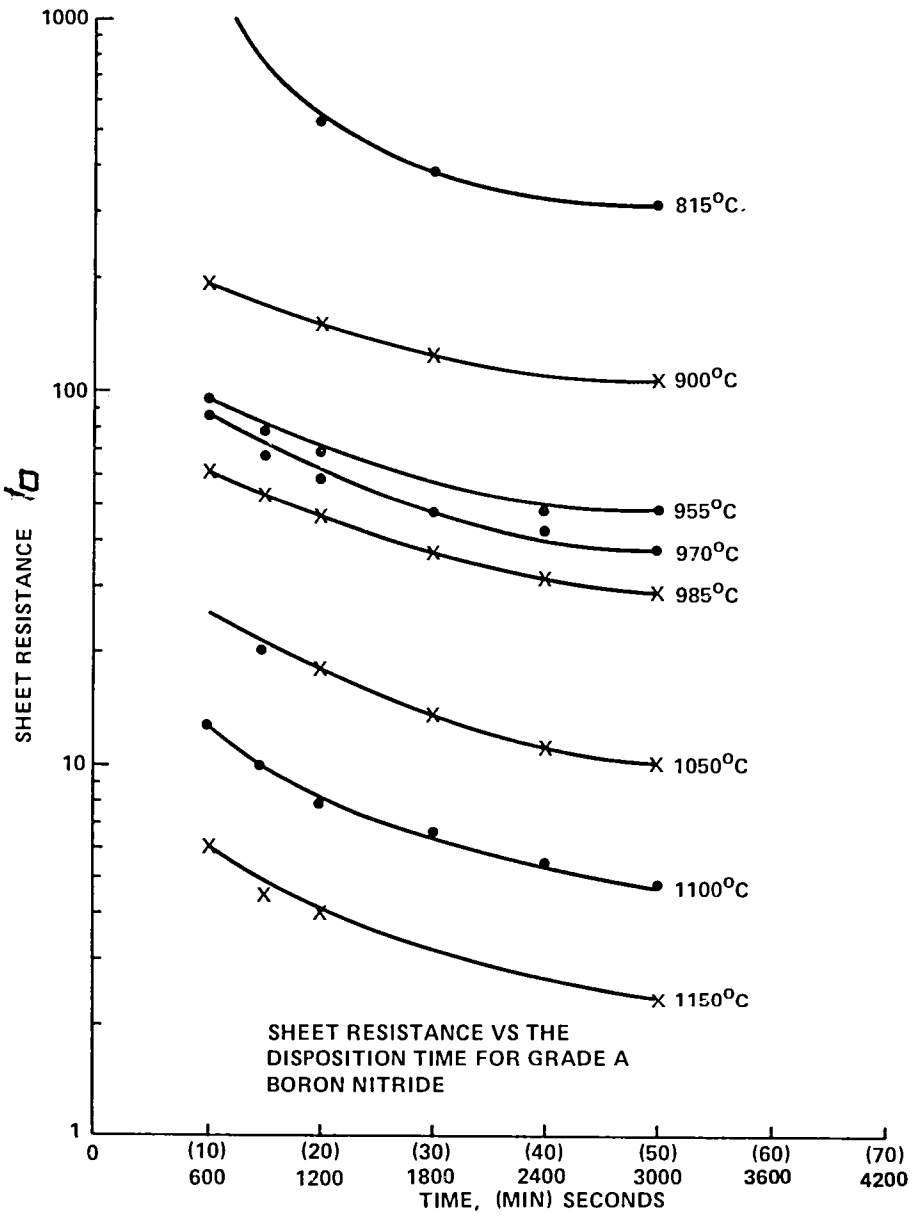


Figure C-1. Boron nitride diffusion curves, sheet resistivity versus deposition time at various temperatures

APPENDIX D

BORON OXIDE DIFFUSIONS

Boron oxide (P+) diffusions are primarily dependent upon time and temperature. Figure D-1 presents sheet resistivity versus deposition time at various temperatures. Sheet resistance is defined in units of ohms per square unit of area (□) because it is a function of geometry.

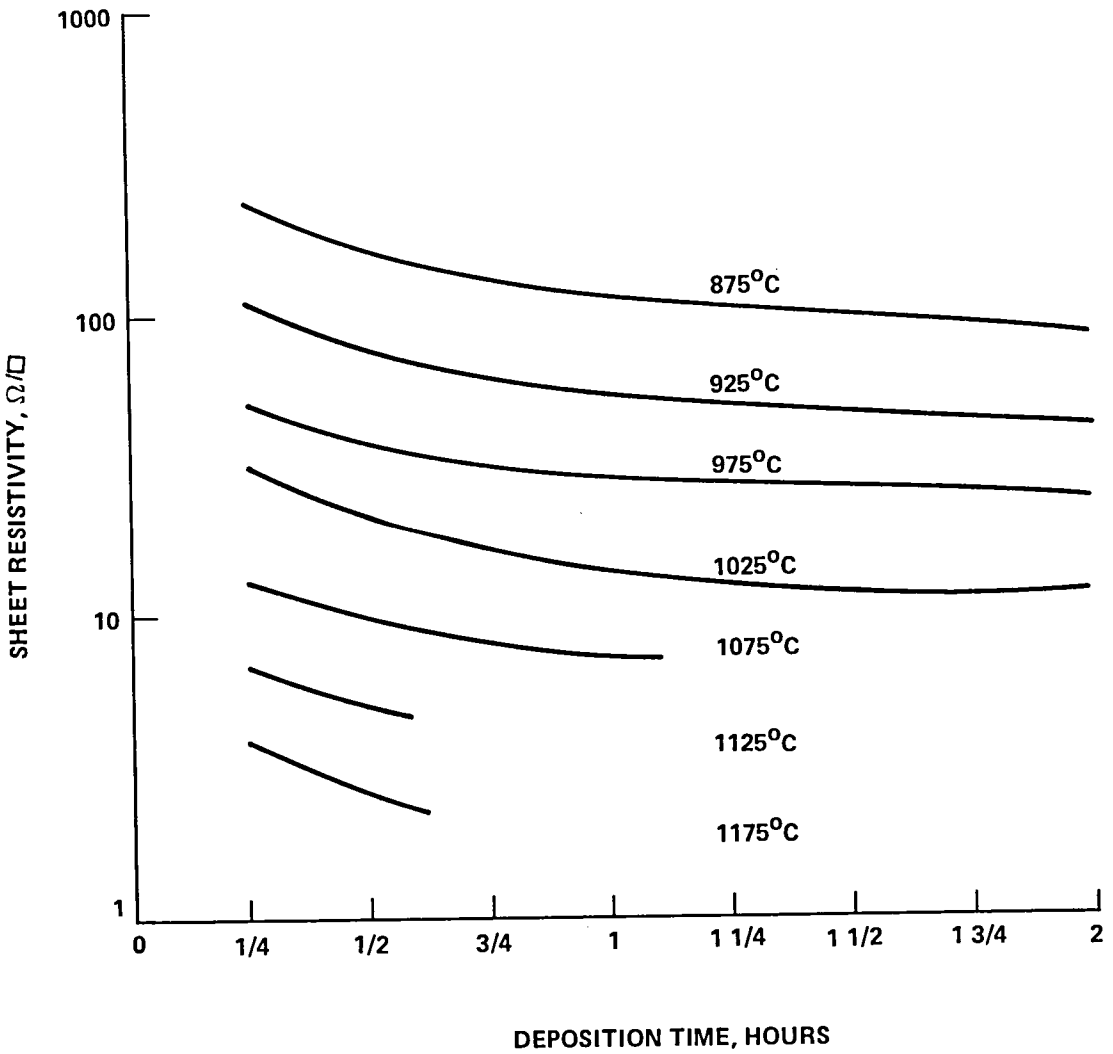


Figure D-1. Boron oxide diffusion curves, sheet resistivity versus deposition time at various temperatures, boron oxide.

APPENDIX E

OXIDE ETCH RATES

Silicon dioxide can be etched by hydroflouric acid which is the main ingredient in most oxide etchants. The two oxide etchants containing HF used in this C-MOS process are the HF solution and the buffered oxide etchant described in Appendix A. HF solution is used when careful control of the thickness of oxide to be etched is required. At 294°K (21°C), HF solution etches at approximately 0.5 nm/s. Buffered oxide etchant is used at 323°K (50°C) for the contact cutout etch to produce "controlled undercutting" needed to make smooth slopes in the oxide so crossing metal interconnects will not encounter abrupt edges. The etch rate versus temperature is given in Figure E-1.

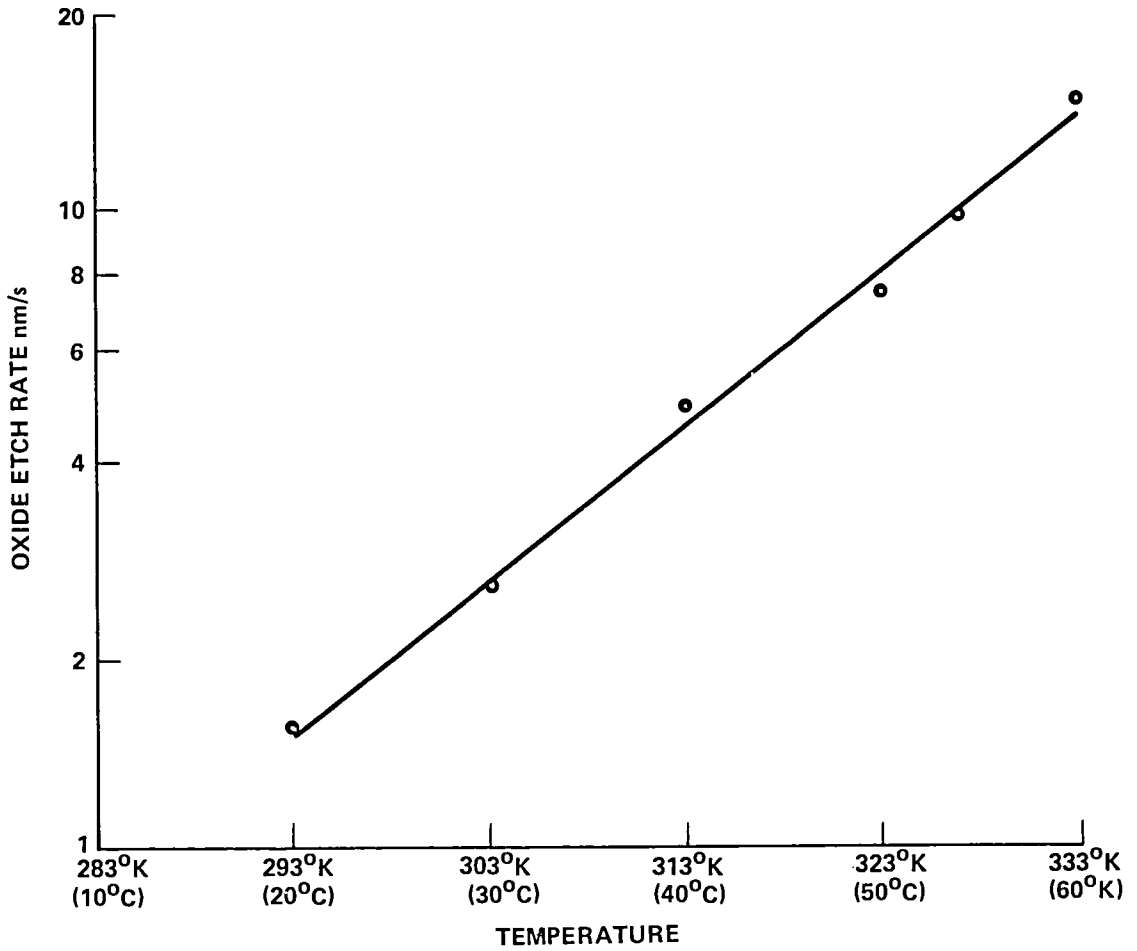


Figure E-1. Silicon Dioxide Etch Rate Versus Temperature

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16. ABSTRACT

The fabrication techniques and procedure details for creation of Complementary Metal Oxide Semiconductor integrated circuits at George C. Marshall Space Flight Center are described. A unique feature of the MSFC process has been included, i.e., the use of multilevel metal interconnect patterns. Examples of C-MOS integrated circuits fabricated at MSFC with functional descriptions of each are given. Typical electrical characteristics of both P-channel Metal Oxide Semiconductor and N-channel Metal Oxide Semiconductor discrete devices under given conditions are provided. A general description of MSFC design, mask making, packaging, and testing procedures is included.

The capabilities described in this report are being utilized in: (1) research and development of new technology, (2) education of individuals in the various disciplines and technologies in the field of microelectronics, and (3) fabrication of many types of specially designed integrated circuits, which are not commercially feasible in small quantities, for in-house research and development programs.

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